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(54) **COMPENSATION OF THRESHOLD VOLTAGE IN DRIVING TRANSISTOR OF ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE**

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(57) **ABSTRACT**

The organic light emitting diode display device comprising a display panel a plurality of pixels arranged in a matrix form, each of the pixels comprising: a driving TFT including a gate electrode coupled to a first node, a source electrode coupled to a second node, and a drain electrode coupled to a high-potential voltage line; an organic light emitting diode including an anode coupled to the second node and a cathode coupled to a low-potential voltage line; a first TFT supplying a data voltage to the first node in response to a scan signal; a initialization control circuit initializing the first node to a first reference voltage and the second node or the third node to a second reference voltage in response to a initialization signal and an emission signal; and capacitors.

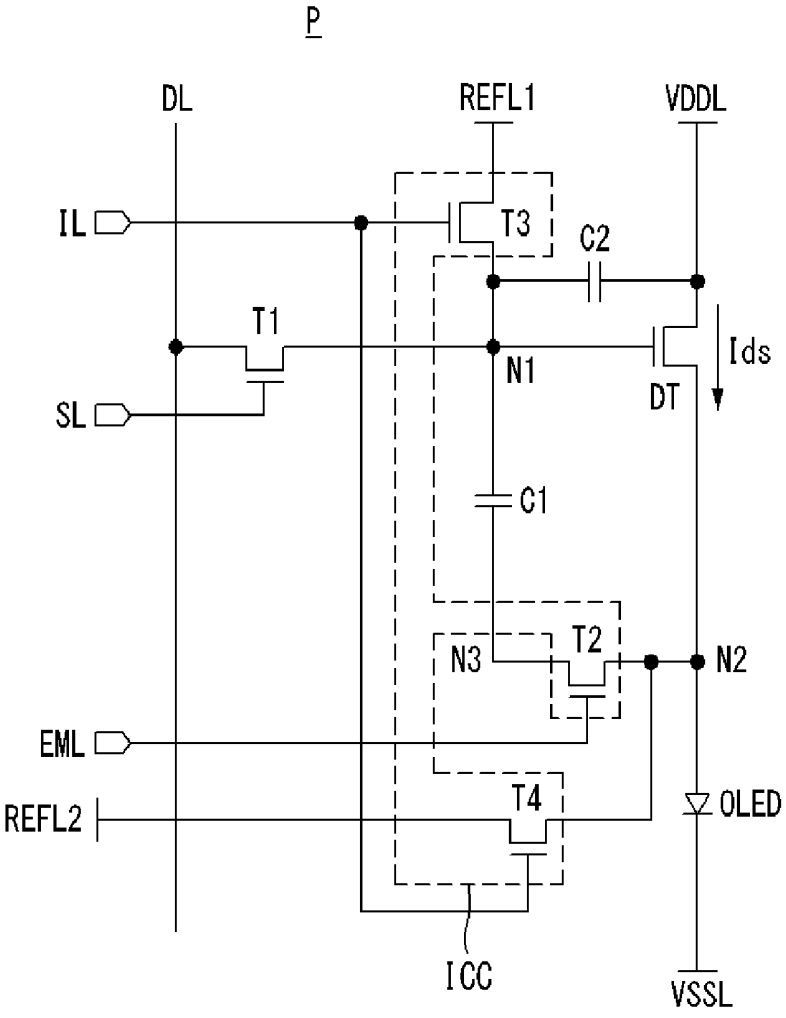


FIG. 1

(PRIOR ART)

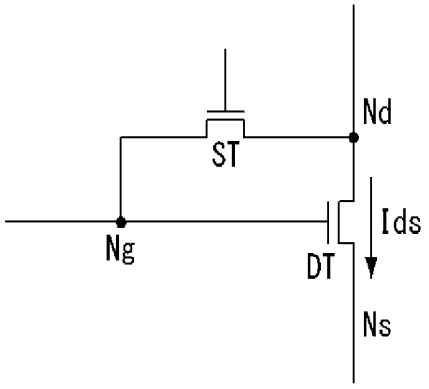
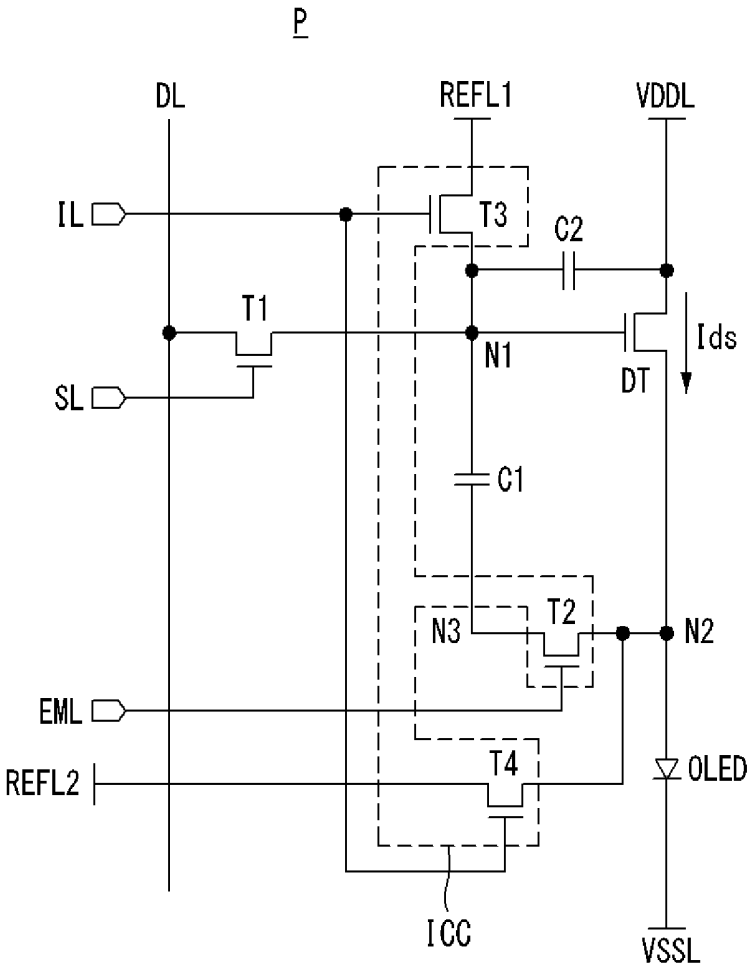


FIG. 2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T3
C2
T1
N1
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DT
SL
C1
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N2
EML
T4
OLED
REFL2
ICC
VSSL

FIG. 3

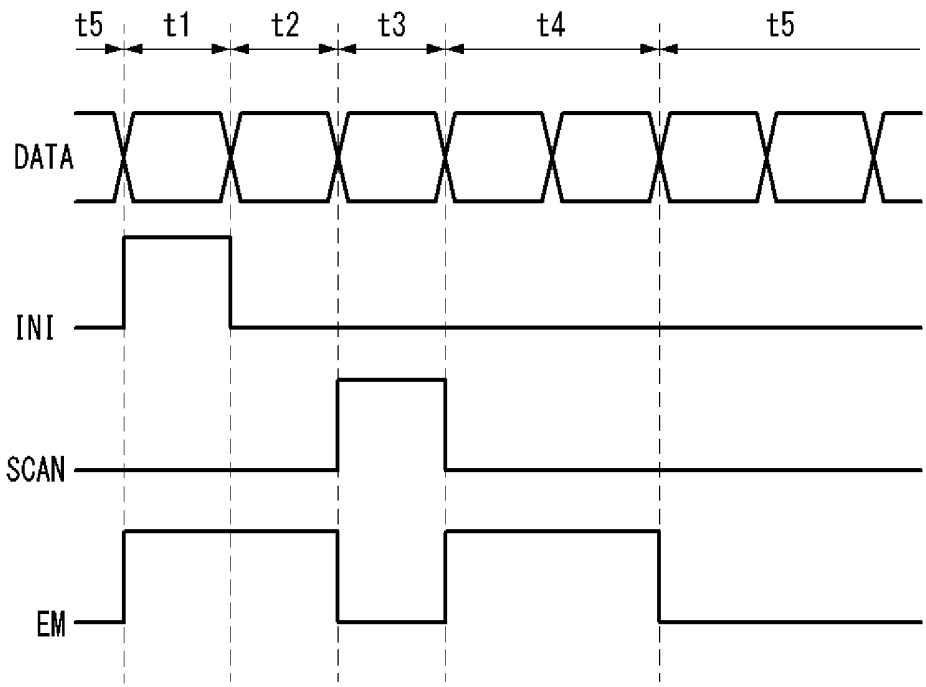
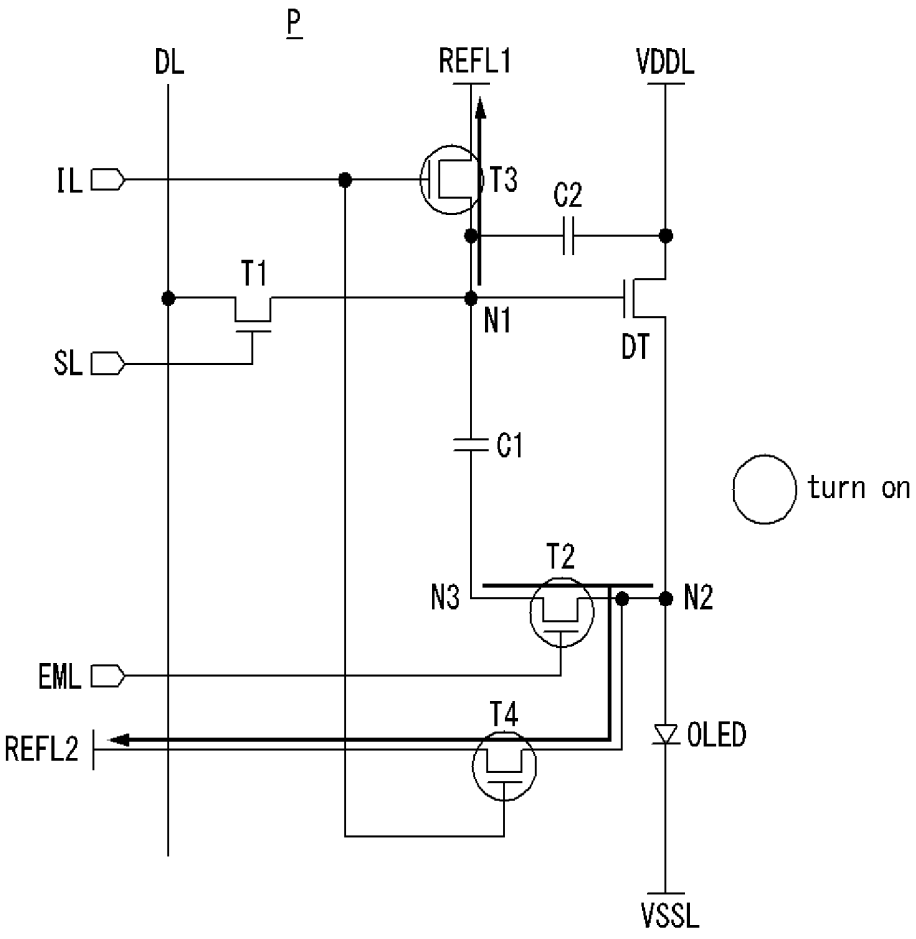


FIG. 4

Period	N1	N2	N3
t1	REF1	REF2	REF2
t2	A	A - Vth	A - Vth
t3	DATA	A - Vth	A - Vth - (A - DATA)
t4	DATAxC2+C1(Vth+Voled_anode) / (C1+C2)	Voled_anode	Voled_anode

FIG. 5A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IL
T3
C2
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N1
DT
SL
C1
turn on
T2
N3
N2
EML
T4
OLED
REFL2
VSSL

FIG. 5B

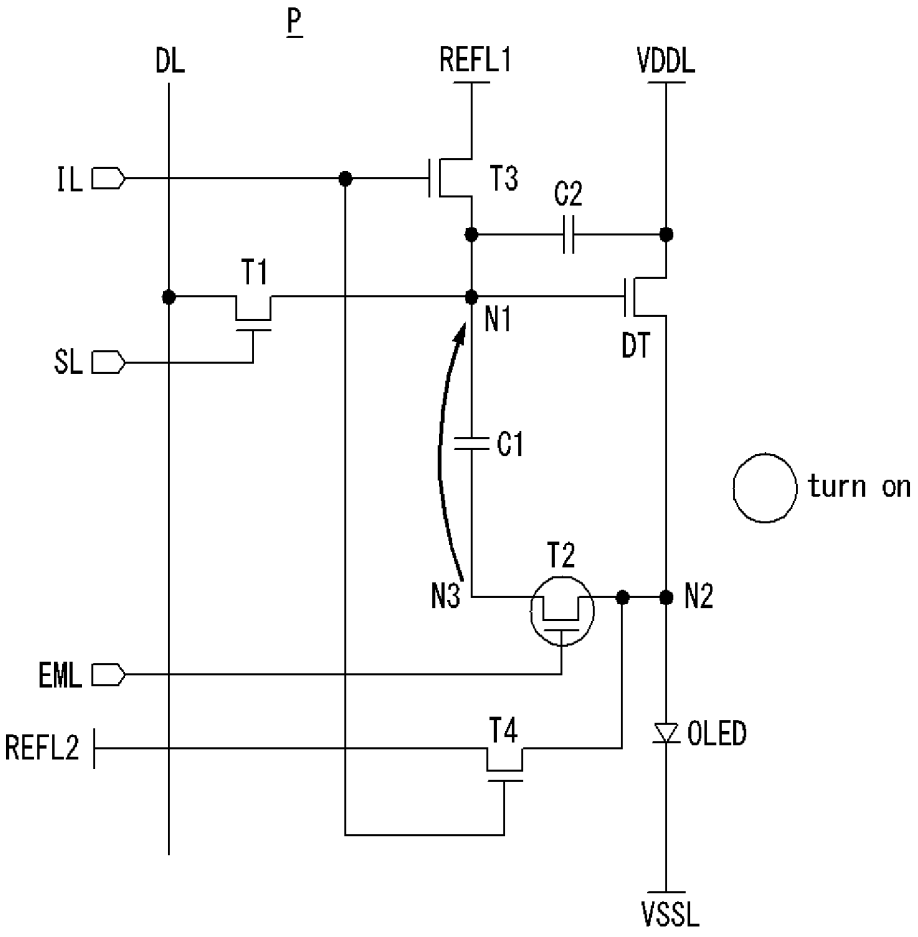
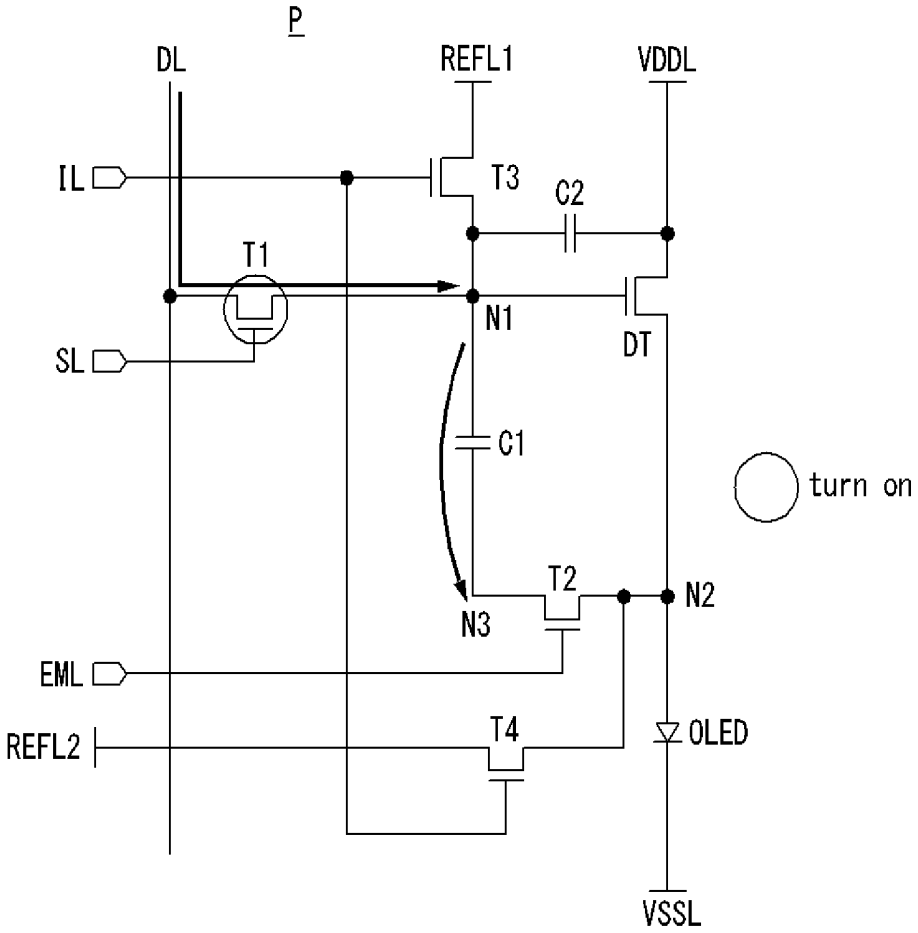

P
DL
REFL1
VDDL
IL
T3
C2
T1
N1
DT
SL
C1
turn on
T2
N3
N2
EML
REFL2
T4
OLED
VSSL

FIG. 5C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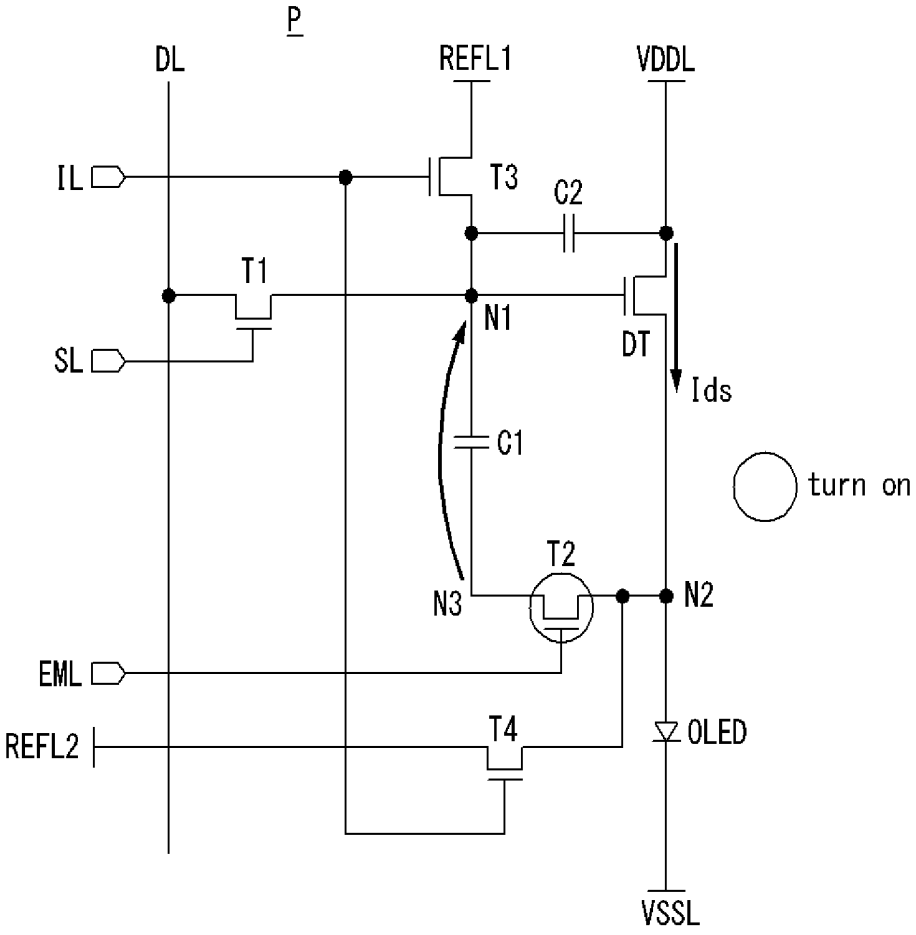
T3
C2
T1
N1
DT
SL
C1
turn on
T2
N2
N3
EML
REFL2
T4
OLED
VSSL

FIG. 5D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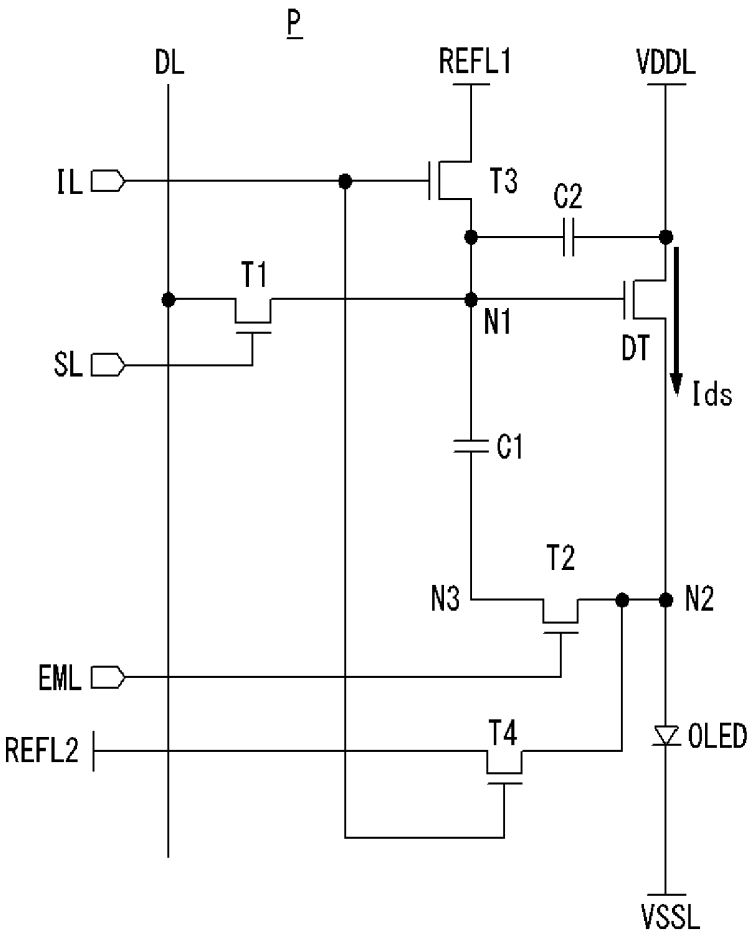
T3
C2
T1
N1
DT
SL
Ids
C1
turn on
T2
N3
N2
EML
REFL2
T4
OLED
VSSL

FIG. 5E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T3
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N1
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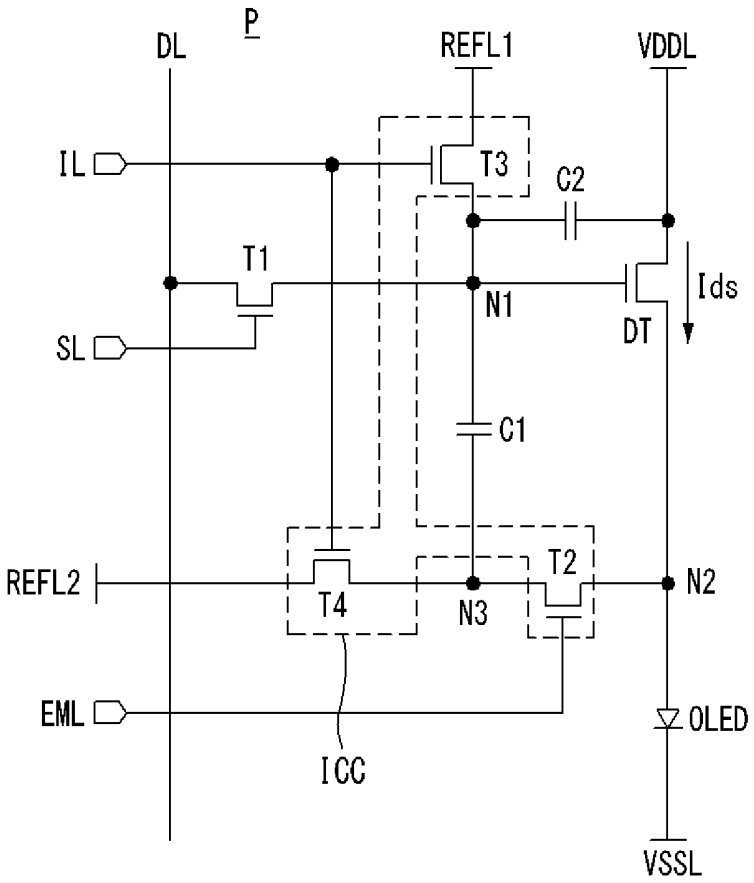
Ids
C1
T2
N3
N2
EML
REFL2
T4
OLED
VSSL

FIG. 6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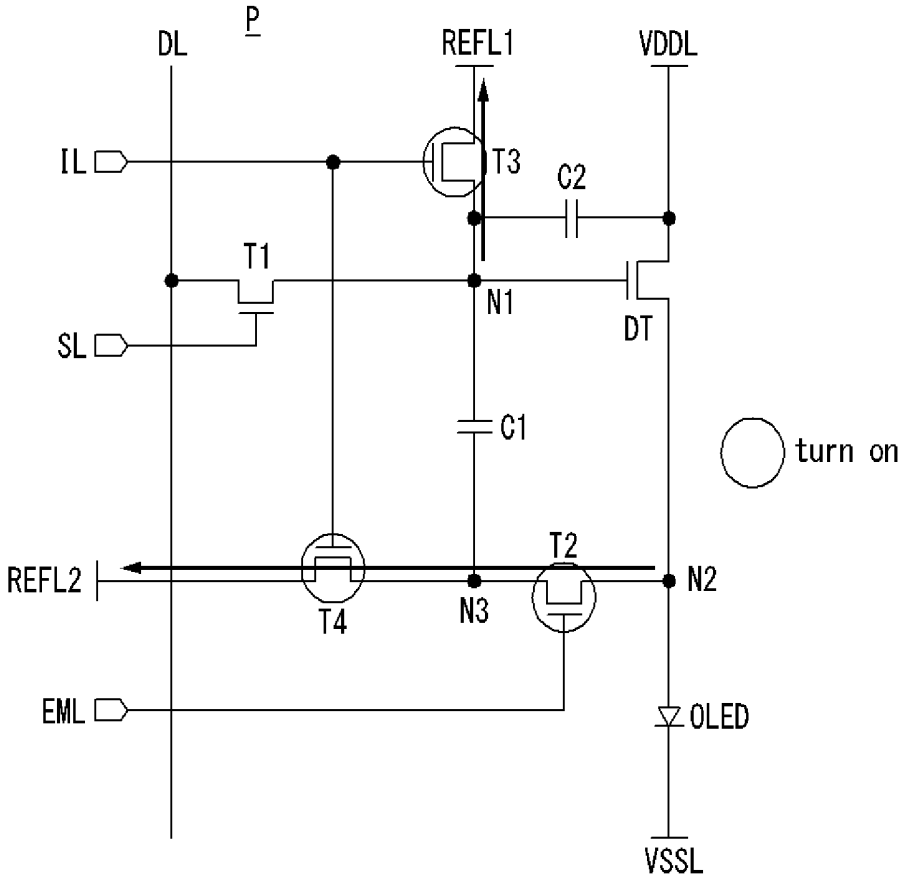
C2
T1
N1
Ids
DT
SL
C1
REFL2
T4
N3
T2
N2
EML
OLED
ICC
VSSL

FIG. 7

Period	N1	N2	N3
t1	REF1	REF2	REF2
t2	A	A - Vth	A - Vth
t3	DATA	A - Vth	A - Vth - (A - DATA)
t4	DATAxC2+C1(Vth+Voled_anode) / (C1+C2)	Voled_anode	Voled_anode

FIG. 8A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IL
T3
C2
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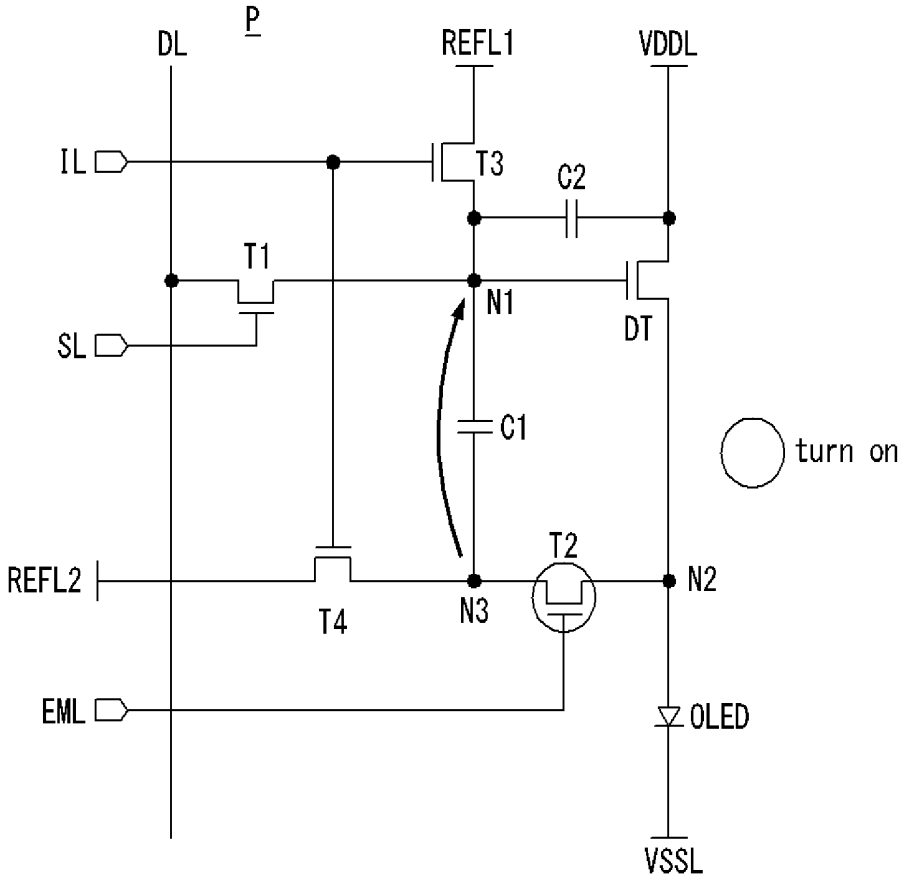
N1
DT
SL
C1
turn on
T2
REFL2
T4
N3
N2
EML
OLED
VSSL

FIG. 8B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IL
T3
C2
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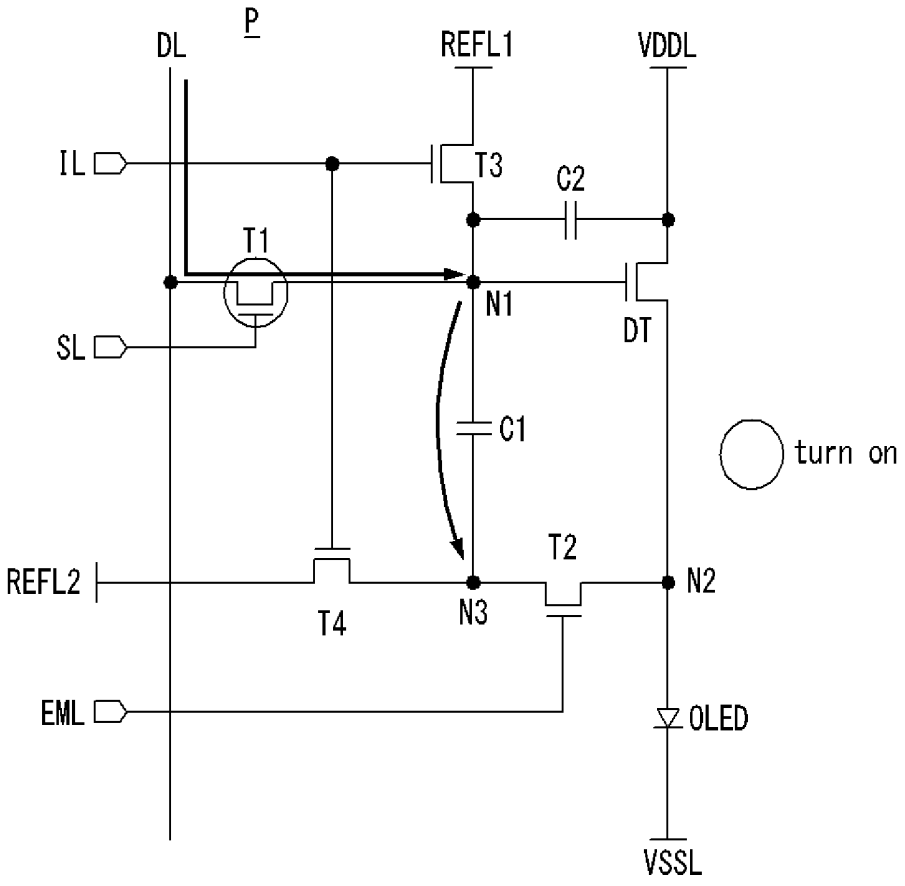
N1
DT
SL
C1
turn on
T2
REFL2
T4
N3
N2
EML
OLED
VSSL

FIG. 8C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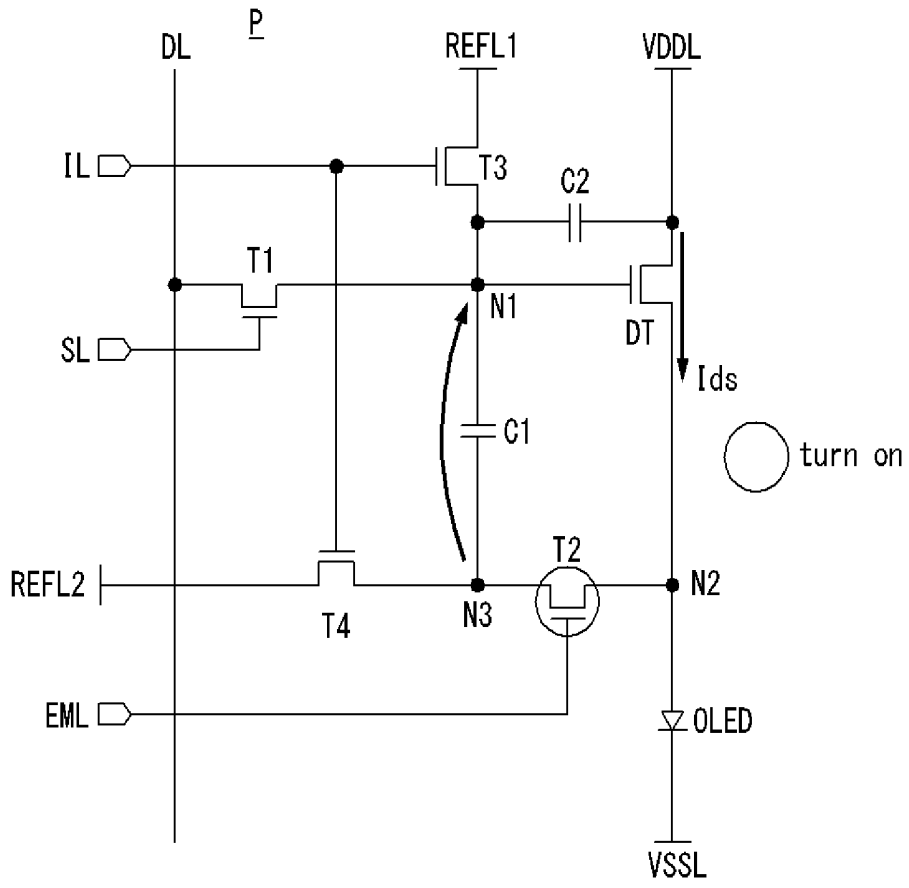
REFL1
VDDL
IL
T3
C2
T1
N1
DT
SL
C1
turn on
T2
REFL2
T4
N3
N2
EML
OLED
VSSL

FIG. 8D


P
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VDDL
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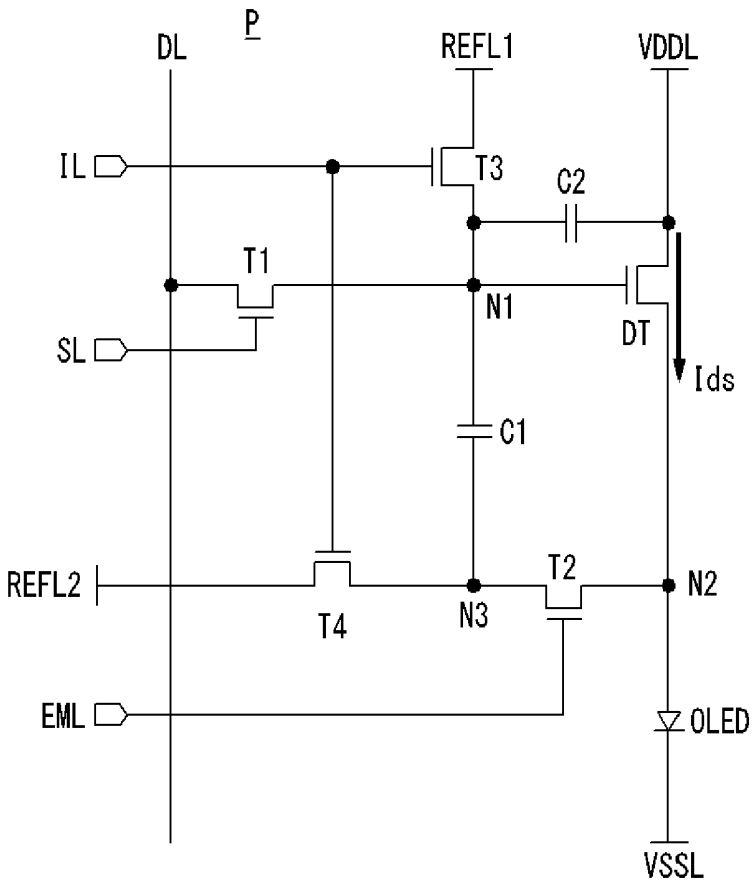
T3
C2
T1
N1
DT
SL
Ids
C1
turn on
T2
REFL2
N2
T4
N3
EML
OLED
VSSL

FIG. 8E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T3
C2
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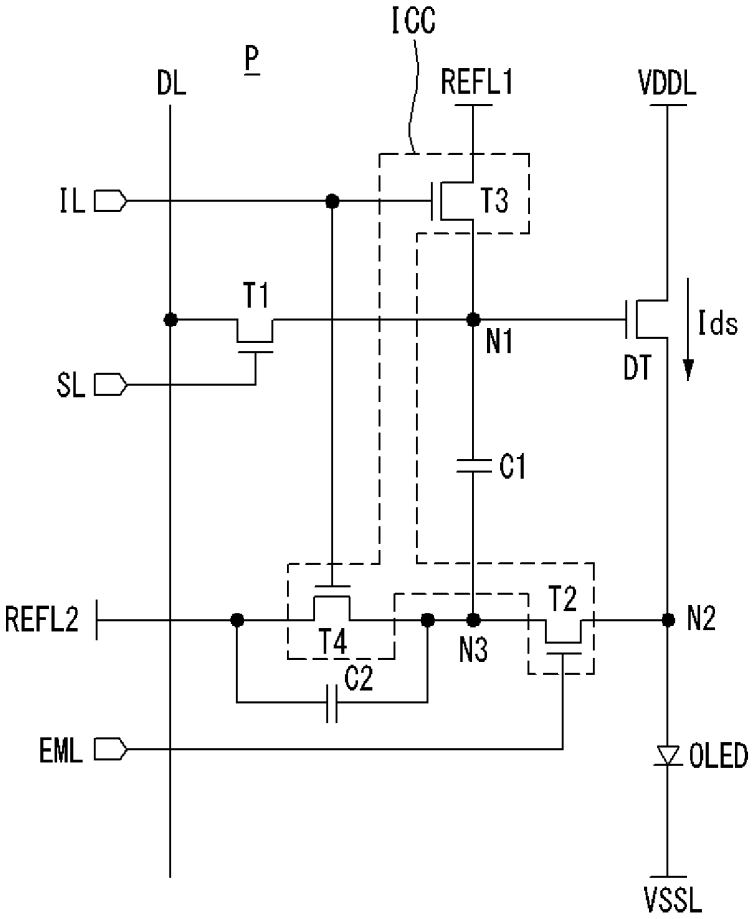
DT
SL
Ids
C1
REFL2
T4
N3
T2
N2
EML
OLED
VSSL

FIG. 9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T3
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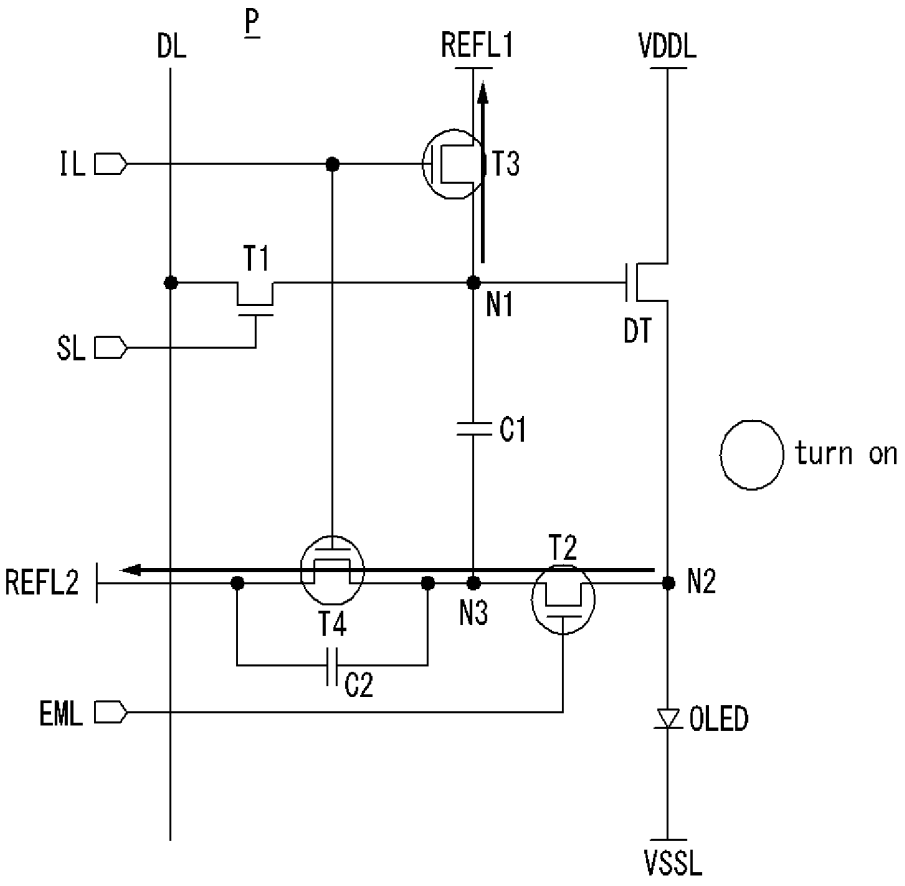
N1
SL
DT
C1
T2
REFL2
T4
N3
N2
C2
EML
OLED
VSSL

FIG. 10

Period	N1	N2	N3
t1	REF1	REF2	REF2
t2	A	A - Vth	A - Vth
t3	DATA	A - Vth	A - Vth - (A - DATA) x C'
t4	DATA+(Voled_anode - [A' - Vth - (A' - DATA) x C'])	Voled_anode	Voled_anode

FIG. 11A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T1
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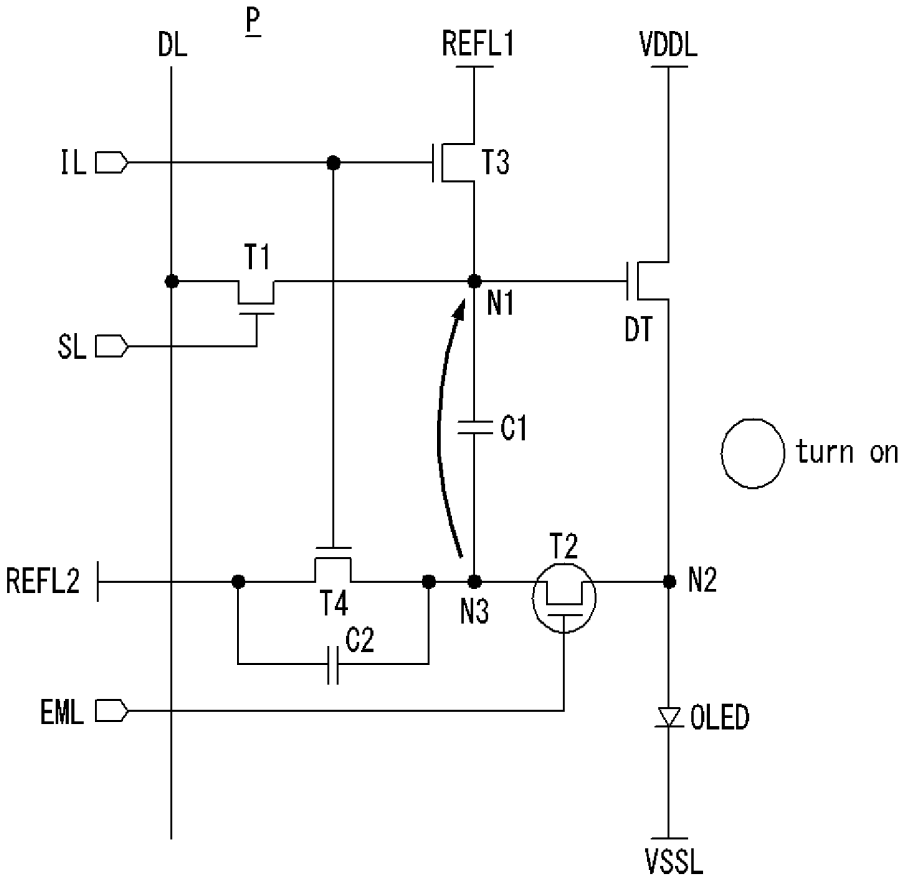
DT
SL
C1
turn on
T2
REFL2
N2
T4
N3
C2
EML
OLED
VSSL

FIG. 11B


P
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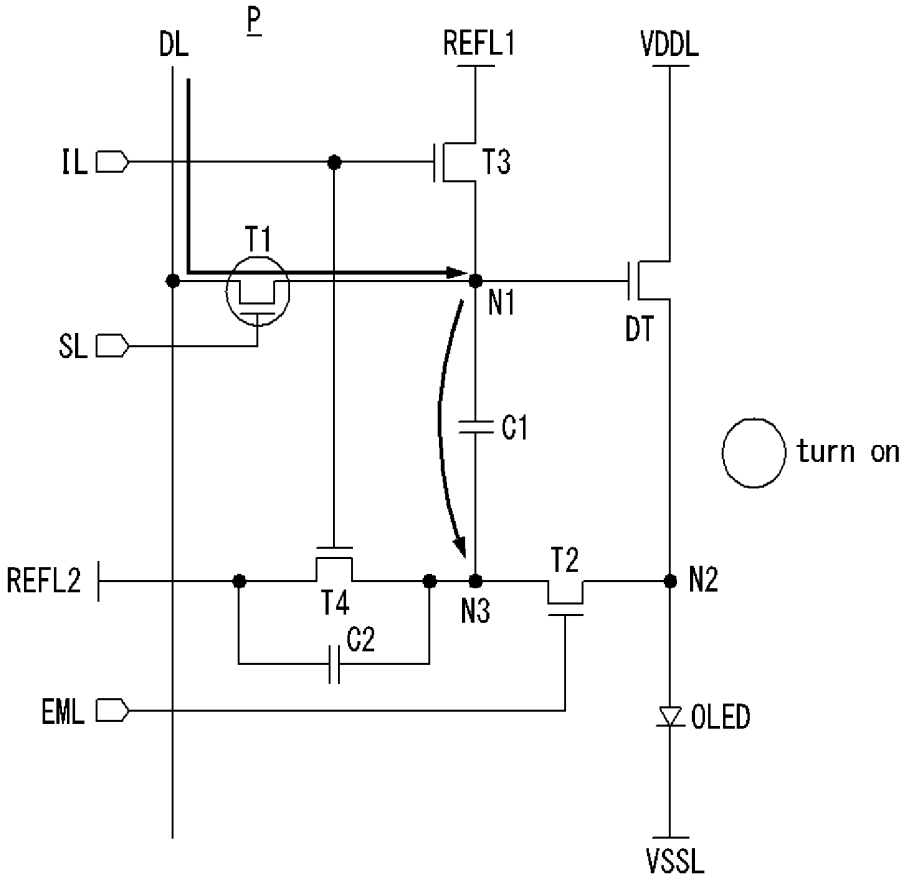
REFL1
VDDL
IL
T3
T1
N1
DT
SL
C1
turn on
T2
REFL2
T4
N3
N2
C2
EML
OLED
VSSL

FIG. 11C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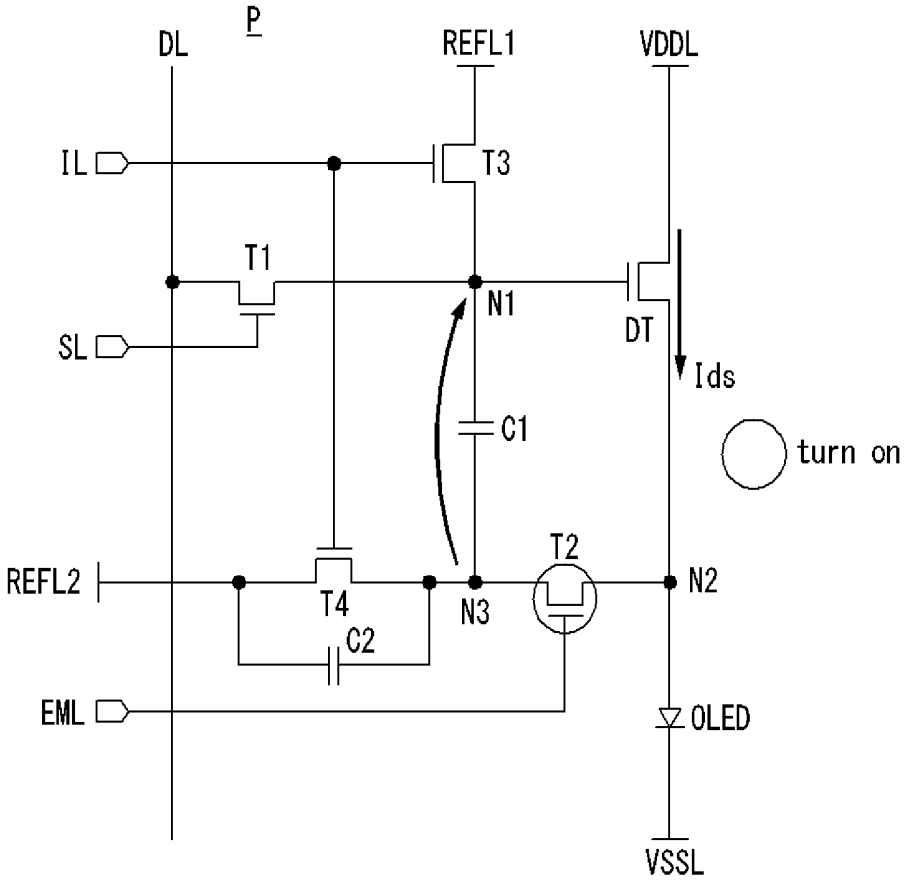
T3
T1
N1
DT
SL
C1
turn on
REFL2
T4
T2
N2
N3
C2
EML
OLED
VSSL

FIG. 11D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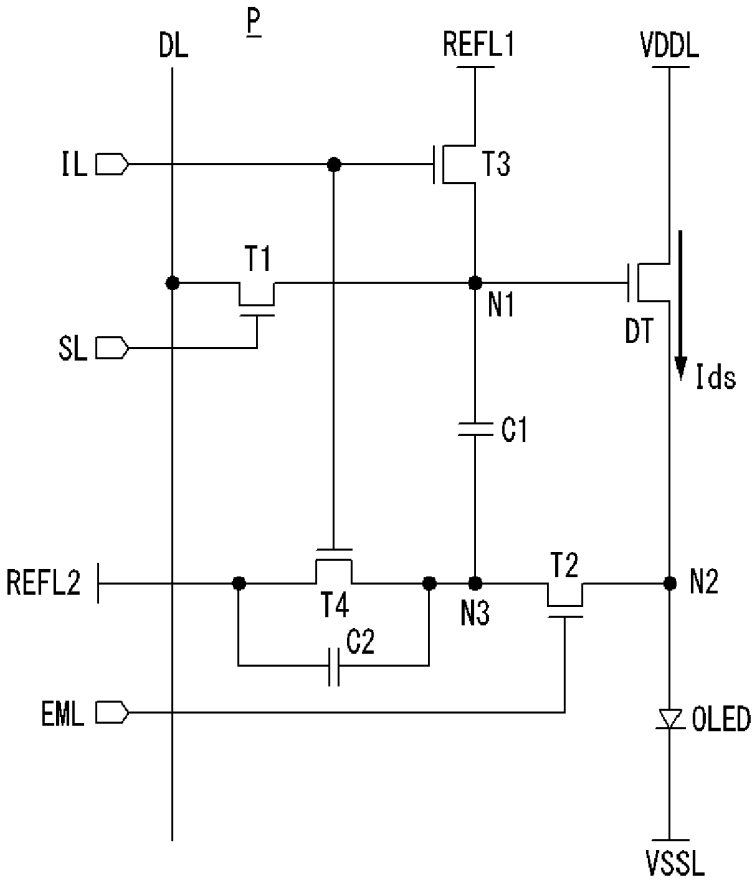
VDDL
IL
T3
T1
N1
DT
SL
Ids
C1
turn on
T2
REFL2
T4
N3
N2
C2
EML
OLED
VSSL

FIG. 11E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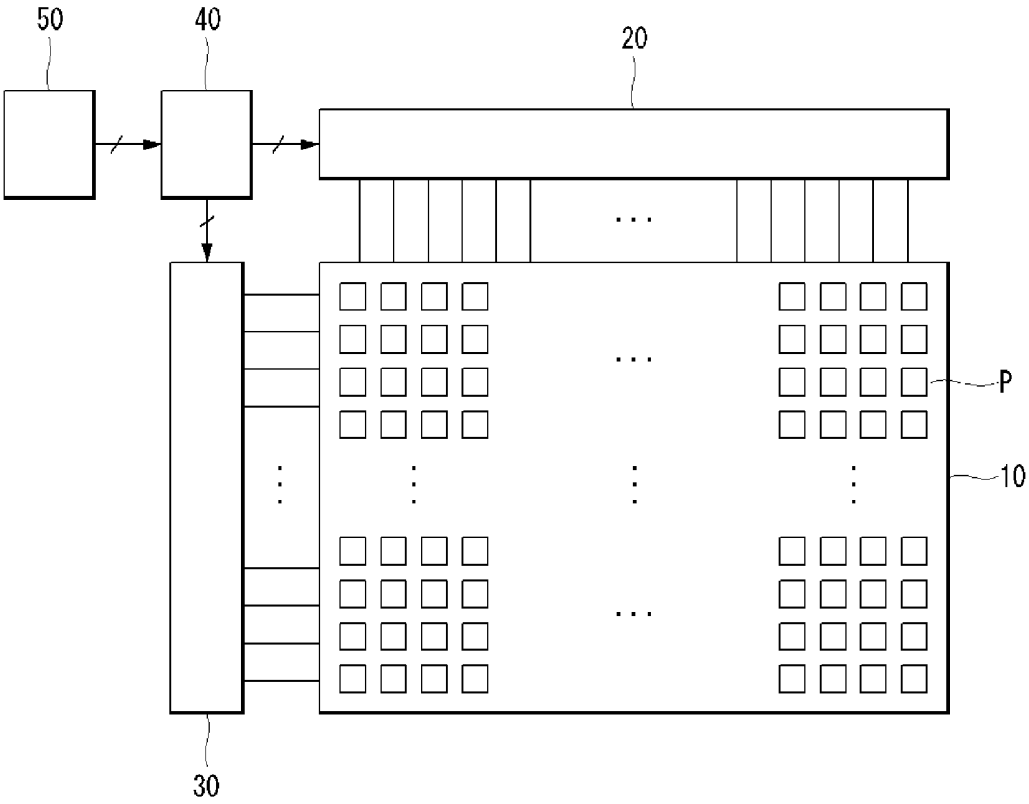
Ids
C1
REFL2
T4
T2
N2
N3
C2
EML
OLED
VSSL

FIG. 12



COMPENSATION OF THRESHOLD VOLTAGE IN DRIVING TRANSISTOR OF ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional application of U.S. patent application Ser. No. 13/865,018 filed on Apr. 17, 2013, which claims priority under 35 U.S.C. §119(a) of Republic of Korea Patent Application No. 10-2012-0083847 filed on Jul. 31, 2012, which are incorporated by reference in their entirety.

BACKGROUND

[0002] 1. Technical Field

[0003] This document relates to an organic light emitting diode display device compensating the threshold voltage of a driving thin film transistor (TFT).

[0004] 2. Discussion of the Related Art

[0005] With the development of information society, the demand for various types of display devices for displaying an image is increasing. Various flat panel displays such as a liquid crystal display (LCD), a plasma display panel (PDP), and an organic light emitting diode (OLED) have been widely used in recent years. Among the flat panel displays, the organic light emitting diode display device are driven at a low voltage, are thin, have a wide viewing angle and a quick response speed.

[0006] A display panel of the OLED display comprises a plurality of pixels arranged in a matrix form. Each of the pixels comprises a scan thin film transistor (TFT) for supplying a data voltage of a data line in response to a scan signal of a scan line and a driving TFT for adjusting the amount of the current supplied to an organic light emitting diode in accordance with a data voltage supplied to a gate electrode. The drain-source current Ids of the driving TFT supplied to the organic light emitting diode can be expressed by following equation:

$$I_{ds}=k'\cdot(V_{gs}-V_{th})^2 \quad (1)$$

where k' represents a proportionality coefficient determined by the structure and physical properties of the driving TFT, Vgs represents the gate-source voltage of the driving TFT, and Vth represents the threshold voltage of the driving TFT.

[0007] The drain-source current Ids of the driving TFT depends upon the threshold voltage Vth of the driving TFT. However, the threshold voltage Vth of the driving TFT of each of the pixels may have a different value due to a shift in the threshold voltage Vth caused by degradation of the driving TFT. Hence, the current Ids supplied to the organic light emitting diode differs from pixel to pixel even if the same data voltage is supplied to each of the pixels. Accordingly, the luminance of light emitted from the organic light emitting diode of each of the pixels may differ even if the same data voltage is supplied to each of the pixels. To solve this problem, various types of pixel structures for compensating the threshold voltage Vth of the driving TFT have been proposed.

[0008] FIG. **1** is a circuit diagram showing a part of a conventional diode-connected threshold voltage compensation pixel structure. FIG. **1** depicts a driving TFT DT supplying the current to an organic light emitting diode and a sensing TFT ST coupled between a gate node Ng and drain node Nd of the driving TFT DT. The sensing TFT ST allows for a connection between the gate node Ng and drain node Nd of the driving TFT DT during a threshold voltage sensing period of the driving TFT DT so that the driving TFT DT functions as a diode. In FIG. **1**, the driving TFT DT and the sensing TFT ST are illustrated as N-type MOSFET (Metal Oxide Semiconductor Field Effect Transistors).

[0009] Referring to FIG. **1**, the gate node Ng and the drain node Nd are coupled during the threshold voltage sensing period in which the sensing TFT ST is turned on, thereby the gate node Ng and the drain node Nd are in a floating state at substantially the same potential. The floating state refers to a state in which no voltage is supplied to a node, so the node on the floating state affects a voltage change of an adjacent node easily. If a voltage difference Vgs between the gate node Ng and a source node Ns is greater than a threshold voltage, the driving TFT DT forms a current path until the voltage difference Vgs between the gate node Ng and the source node Ns reaches the threshold voltage Vth of the driving TFT DT, and as a result, the voltage of the gate node Ng and the voltage of the drain node Nd are lowered. However, if the threshold voltage Vth of the driving TFT DT is shifted to a negative voltage, the voltage difference Vgs between the gate node Ng and the source node Ns cannot reach the threshold voltage Vth of the driving TFT DT, even if the voltage at the gate node Ng goes down to the voltage at the source node Ns, because the threshold voltage Vth of the driving TFT DT is lower than 0 V. Consequently, if the threshold voltage Vth of the driving TFT DT is shifted to a negative voltage, it is impossible to sense the threshold voltage Vth of the driving TFT DT correctly. A negative shift refers to shifting the threshold voltage Vth of the driving TFT DT to a voltage lower than 0 V when the driving TFT DT is implemented as an N-type MOSFET. The negative shift usually occurs when a semiconductor layer of the driving TFT DT is formed of an oxide.

SUMMARY

[0010] Embodiments relate to an organic light emitting diode display device including a plurality of pixels arranged in a matrix form. Each of the pixels includes a driving thin film transistor (TFT), an organic light emitting diode, a first TFT, an initialization control circuit and a first capacitor. The driving TFT includes a gate electrode coupled to a first node, a source electrode coupled to a second node, and a drain electrode coupled to a high-potential voltage line. The organic light emitting diode is placed between the second node and a low-potential voltage line. The first TFT is configured to connect a data line to the first node during a data voltage supply period of a frame period. The initialization control circuit is coupled between the first node and a first reference voltage line supplying a first reference voltage and is connected to a second node, a third node and a second reference voltage line supplying a second reference voltage. The initialization control circuit is configured to initialize the first node to the first reference voltage, and the second and third nodes are initialized to a second reference voltage during an initialization period of the frame period preceding the data voltage supply period. The first capacitor is coupled between the first node and the third node. The first capacitor is configured to store a voltage difference between the first node and the third node during the initialization period, and change a voltage level of the first node based on a voltage level of the third node in a threshold voltage sensing period between the initialization period and the data voltage supply period.

[0011] The features and advantages described in this summary and the following detailed description are not intended to be limiting. Many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a circuit diagram showing a part of a conventional diode-connected threshold voltage compensation pixel structure;

[0013] FIG. **2** is an equivalent circuit diagram of a pixel according to a first exemplary embodiment.

[0014] FIG. **3** is a waveform diagram showing signals which are input into a pixel according to an exemplary embodiment.

[0015] FIG. **4** is a table showing changes in the voltages of nodes of a pixel according to a first exemplary embodiment.

[0016] FIGS. **5**A to **5**E are circuit diagrams of a pixel according to a first exemplary embodiment during first to fifth periods.

[0017] FIG. **6** is a circuit diagram of a pixel according to a second exemplary embodiment.

[0018] FIG. **7** is a table showing changes in the voltages of nodes of a pixel according to a second exemplary embodiment.

[0019] FIGS. **8**A to **8**E are circuit diagrams of a pixel according to a second exemplary embodiment during first to fifth periods.

[0020] FIG. **9** is a circuit diagram of a pixel according to a third exemplary embodiment.

[0021] FIG. **10** is a table showing changes in the voltages of nodes of a pixel according to a third exemplary embodiment.

[0022] FIGS. **11**A to **11**E are circuit diagrams of a pixel according to a third exemplary embodiment of first to fifth periods.

[0023] FIG. **12** is a block diagram schematically showing an organic light emitting diode display device according to an exemplary embodiment.

DETAILED DESCRIPTION

[0024] Embodiments will be described more fully hereinafter with reference to the accompanying drawings. Like reference numerals designate like elements throughout the specification. In the following description, if it is decided that the detailed description of known function or configuration related to the embodiments make the subject matter unclear, the detailed description is omitted.

[0025] A pixel of an organic light emitting diode display device according to an exemplary embodiment may internally compensate the threshold voltage of a driving TFT. Internal compensation refers to sensing and compensating the threshold voltage of the driving TFT in real time within the pixel.

[0026] FIG. **2** is a circuit diagram of a pixel according to a first exemplary embodiment. Referring to FIG. **2**, the pixel P according to the first exemplary embodiment comprises a driving TFT (thin film transistor) DT, an organic light emitting diode (OLED), a control circuit, and capacitors.

[0027] The driving TFT DT adjusts the amount of drain-source current Ids according to the level of a voltage applied to a gate electrode. The gate electrode of the driving TFT DT is coupled to a first node N**1**, a source electrode thereof is coupled to a second node N**2**, and a drain electrode thereof is coupled to a high-potential voltage line VDDL supplying a high-potential voltage VDD.

[0028] An anode of the organic light emitting diode is coupled to the second node N**2**, a cathode thereof is coupled to a low-potential voltage line VSSL supplying a low-potential voltage VSS. The organic light emitting diode OLED emits light depending on the drain-source current Ids of the driving TFT DT.

[0029] The control circuit comprises a first TFT T**1** and an initialization control circuit ICC. The first TFT T**1** is a scan TFT which supplies a data voltage DATA of a data line DL to the first node N**1** in response to a scan signal SCAN supplied through a scan line SL. A gate electrode of the first TFT T**1** is coupled to the scan line SL, a source electrode thereof is coupled to the first node N**1**, and a drain electrode thereof is coupled to the data line DL.

[0030] The initialization control circuit (ICC) includes second to fourth TFT T**2** through T**4**. The second TFT T**2** is a node connection control TFT which controls to connect the second node N**2** to the third node N**3** in response to an emission signal EM supplied through an emission line EML. A gate electrode of the second TFT T**2** is coupled to the emission line EML, a source electrode thereof is coupled to the third node N**3**, and a drain electrode thereof is coupled to the second node N**2**. The third TFT T**3** is a first initialization TFT which initializes the first node N**1** to a first reference voltage REF**1** supplied through a first reference voltage line REFL**1** in response to an initialization signal INI supplied through an initialization line IL. A gate electrode of the third TFT T**3** is coupled to the initialization line IL, a source electrode thereof is coupled to the first reference voltage line REFL**1**, and a drain electrode thereof is the first node N**1**. The fourth TFT T**4** is a second initialization TFT which initializes the second node N**2** to a second reference voltage REF**2** supplied through a second reference voltage line REFL**2** in response to the initialization signal INI. A gate electrode of the third TFT T**4** is coupled to the initialization line IL, a source electrode thereof is coupled to the second reference voltage line REFL**2**, and a drain electrode thereof is the second node N**2**.

[0031] The first capacitor C**1** is coupled between the first node N**1** and the third node N**3**. The first capacitor C**1** stores a differential voltage between a voltage at the first node N**1** and a voltage at the third node N**3**. The second capacitor C**2** is coupled between the first node N**1** and the high-potential voltage line VDDL. In this case, the second capacitor C**2** stores a differential voltage between a voltage at the first node N**1** and the high potential voltage VDD. Or, the second capacitor C**2** may be coupled between the first node N**1** and the first reference voltage line REFL**1**. In this case, the second capacitor C**2** stores a differential voltage between the first reference voltage REF**1**. Alternatively, the second capacitor C**2** may be coupled between the first node N**1** and the second reference voltage line REFL**2**. In this case, the second capacitor C**2** stores a differential voltage between a voltage at the first node N**1** and the second reference voltage REF**2**.

[0032] The first node N**1** is a contact point at which the gate electrode of the driving TFT DT, the source electrode of the first TFT T**1**, the drain electrode of the third TFT T**3**, one electrode of the first capacitor C**1**, and one electrode of the second capacitor C**2** are coupled. The second node N**2** is a contact point at which the source electrode of the driving TFT DT, the anode of the organic light emitting diode, the drain electrode of the second TFT T**2**, and the drain electrode of the

fourth TFT T4 are coupled. The third node N3 is a contact point at which the source electrode of the second TFT T2 and the other electrode of the first capacitor C1 are coupled.

[0033] Semiconductor layers of the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT DT have been described as being formed of an oxide semiconductor. However, the embodiments are not limited thereto, and the semiconductor layers of the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT DT may be formed of either a-Si or Poly-Si. Also, the exemplary embodiment has been described with respect to an example in which the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT DT are implemented as N-type MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). However, the present invention is not limited thereto, but the first to fourth TFTs T1, T2, T3, and T4 and the driving TFT DT are implemented as P-type MOSFETs.

[0034] After consideration of the characteristics of the driving TFT DT and the characteristics of the organic light emitting diode OLED, the high-potential voltage source is set to supply the high-potential voltage VDD through the high-potential voltage line VDDL, and the low-potential voltage source is set to supply the low-potential voltage VSS through the low-potential voltage line VSSL. For example, the high-potential voltage VDD may be set to approximately 20V, the low-potential voltage VSS may be set to approximately 0V. Also, the first reference voltage source is set to supply the first reference voltage REF1 through the first reference voltage line REFL1, and the second reference voltage source is set to supply the second reference voltage REF2 through the second reference voltage line REFL2. The second reference voltage REF2 is lower than a difference voltage between the first reference voltage REF1 and the threshold voltage Vth of the driving TFT DT to sense the threshold voltage Vth of the driving TFT DT.

[0035] FIG. 3 is a waveform diagram showing signals received at a pixel according to an exemplary embodiment. FIG. 3 depicts an initialization signal INI supplied to an initialization line IL, a scan signal SCAN supplied to a scan line SL, and an emission signal EM supplied to an emission line EML. Also, FIG. 3 depicts a data voltage DATA supplied to a data line DL.

[0036] With reference to FIG. 3, the initialization signal INI, the scan signal SCAN, and the emission signal EM are signals for controlling first to fourth TFTs T1, T2, T3, and T4. Each of the initialization signal INI, the scan signal SCAN, and the emission signal EM is generated as a cycle of one frame period. Each of the initialization signal INI, the scan signal SCAN, and the emission signal EM swings between a first logic level voltage and a second logic level voltage. For example, the first logic level voltage is implemented as a gate high voltage VGH and the second logic level voltage is implemented as a gate low voltage VGL as shown in FIG. 3. The gate high voltage VGH is set to approximately 14V to 20V, and the gate low voltage VGL is set to approximately −5V to −12V.

[0037] One frame period is divided into first to fifth periods t1, t2, t3, t4, and t5. A first period t1 is an initialization period that initializes first to third nodes N1, N2, and N3. A second period t2 is a threshold voltage sensing period that senses a threshold voltage Vth of a driving TFT DT. A third period t3 is a data voltage supply period that supplies a data voltage DATA to a first node N1. A fourth period t4 and a fifth period t5 are an emission period that emits an organic light emitting diode OLED depending on the drain-source current Ids of the driving TFT DT.

[0038] The initialization signal INI and the emission signal EM are generated as the gate high voltage VGH, and the scan signal SCAN is generated as the gate low voltage VGL during the first period t1. The emission signal EM is generated as the gate high voltage VGH, and the scan signal SCAN and the emission signal EM are generated as the gate low voltage VGL during the second period t2. The scan signal SCAN is generated as the gate high voltage VGH, and the initialization signal INI and the emission signal EM are generated as the gate low voltage VGL during the third period t3. The emission signal EM is generated as the gate high voltage VGH, and the initialization signal INI and the scan signal SCAN are generated as the gate low voltage VGL during the fourth period t4. The initialization signal INI, the scan signal SCAN, and the emission signal EM are generated as the gate low voltage VGL during the fifth period t5.

[0039] The data voltage DATA is generated every horizontal period 1H. In the embodiment of FIG. 3, the third period t3 that supplies the data voltage DATA to the first node N1 is generated as one horizontal period 1H. However, other arrangements may be used in other embodiments. That is, the first to fourth periods t1, t2, t3, and t4 are several horizontal periods or dozens of horizontal periods for improving a picture quality of each pixel. Meanwhile, one horizontal period refers to one line scanning period in which data voltages are supplied to pixels arranged in one horizontal line of the display panel.

[0040] FIG. 4 is a table showing changes in the voltages of nodes of a pixel according to a first exemplary embodiment. FIGS. 5A through 5E are a circuit diagram of a pixel according to a first exemplary embodiment during first to fifth periods. An operation method of the pixel P will be described in the below with reference to FIGS. 3, 4, and 5A to 5E.

[0041] First, during the first period t1, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate high voltage VGH is supplied through the initialization line IL as shown in FIG. 3. Also, during the first period t1, the emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. 3.

[0042] With reference to FIG. 5A, the first TFT T1 is turned off by the scan signal SCAN having the gate low voltage VGL. The second TFT T2 is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N2 is coupled to the third node N3. The third TFT T3 is turned on in response to the initialization signal INI having the gate high voltage VGH. Therefore, the first node N1 is coupled to the first reference6 voltage line REFL1. The fourth TFT T4 is turned on in response to the initialization signal INI having the gate high voltage VGH. Therefore, the second node N2 is coupled to the second reference voltage line REF2.

[0043] Finally, the voltage of the first node N1 is initialized to the first reference voltage REF1 since the third TFT T3 is turned on. The voltage of the second node N2 is initialized to the second reference voltage REF2 since the fourth TFT T4 is turned on. The voltage of the third node N3 is initialized to the second reference voltage REF2 since the second TFT T2 is turned on.

[0044] Second, during the second period t2, the scan signal SCAN having the gate low voltage VGL is supplied through

the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. **3**. Also, during the second period t**2**, the emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. **3**.

[0045] With reference to FIG. **5**B, the first TFT T**1** is turned off by the scan signal SCAN having the gate low voltage VGL. The second TFT T**2** is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N**2** is coupled to the third node N**3**. The third TFT T**3** and the fourth TFT T**4** are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N**2** and the third node N**3** is no longer coupled to the second reference voltage line REF**2**. Meanwhile, the second node N**2** and the third node N**3** have substantially the same potential since the second TFT T**2** is turned on.

[0046] Because the voltage difference Vgs between the gate and source electrodes of the driving TFT DT is greater than the threshold voltage Vth, the driving TFT DT forms a current path until the voltage difference Vgs between the gate and source electrodes reaches the threshold voltage Vth. Accordingly, the voltage of the second node N**2** rises up. Also, the voltage of the third node N**3** rises up since the second node N**2** is coupled to the third node N**3**. Meanwhile, the voltage change of the third node N**3** is applied to the first node N**1** by the cap boosting of the first capacitor C**1**. If the voltage of the first node N**1** which the voltage change of the third node N**3** is applied to is "A" voltage, the voltage of the second node N**2** rises up to a differential voltage A−Vth between the voltage A of the first node N**1** and the threshold voltage Vth of the driving TFT DT. Also, the voltage of the third node N**3** rises up to a differential voltage A−Vth between the voltage A of the first node N**1** and the threshold voltage Vth of the driving TFT DT because the second node N**2** is coupled to the third node N**3**. "A" voltage may be "REF**1**+α". Finally, the threshold voltage Vth of the driving TFT DT may be stored to the first capacitor C**1** during the second period t**2**.

[0047] Third, during the third period t**3**, the scan signal SCAN having the gate high voltage VGH is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. **3**. Also, during the third period t**3**, the emission signal EM having the gate low voltage VGL is supplied through the emission line EML as shown in FIG. **3**.

[0048] With reference to FIG. **5**C, the first TFT T**1** is turned on in response to the scan signal SCAN having the gate high voltage VGH. Therefore, the first node N**1** is coupled to the data line DL. The second TFT T**2** is turned off by the emission signal EM having the gate low voltage VGL. Therefore, the second node N**2** is no longer coupled to the third node N**3**. The third TFT T**3** and the fourth TFT T**4** are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N**2** and the third node N**3** is not coupled to the second reference voltage line REF**2**. Meanwhile, the data voltage DATA of the data line is supplied to the first node N**1** since the first TFT T**1** is turned on. The third node N**3** is on the floating state since the second TFT T**2** is turned off. The floating state refers to a state on which no voltage is supplied to a node, so the node on the floating state affects voltage change of an adjacent node easily.

[0049] The voltage change of the first node N**1** is applied to the third node N**3** since the third node N**3** is on the floating state during the third period t**3**. Therefore, "A−DATA" corresponding to the voltage change of the first node N**1** is applied to the third node N**3**, thus the voltage of the third node is changed to "A−Vth−(A−DATA)", that is "DATA−Vth".

[0050] Fourth, during the fourth period t**4**, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. **3**. Also, during the fourth period t**4**, the emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. **3**.

[0051] With reference to FIG. **5**D, the first TFT T**1** is turned off by the scan signal SCAN having the gate low voltage VGL. Therefore, the first node N**1** is no longer coupled to the data line DL. The second TFT T**2** is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N**2** is coupled to the third node N**3**. The third TFT T**3** and the fourth TFT T**4** are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N**2** and the third node N**3** is not coupled to the second reference voltage line REF**2**. Meanwhile, the first node N**1** is on the floating state since the first TFT T**1** and the third TFT T**3** are turned off. The second node N**2** and the third node N**3** are at substantially the same potential since the second TFT T**2** is turned on.

[0052] As shown in FIG. **4**, the voltage of the second node N**2** is changed to "Voled_anode" due to the drain-source current Ids of the driving TFT DT according to the voltage of the first node N**1**. Also, the voltage of the third node N**3** is changed to "Voled_anode" because the second node N**2** is coupled to the third node N**3** since the second TFT T**2** is turned on.

[0053] The voltage change of the third node N**3** is applied to the first node N**1** by the first capacitor C**1** because the first node N**1** is on the floating state during the fourth period t**4**. Therefore, the voltage change of the third node N**3**, "DATA−Vth−Voled_anode" is applied to the first node N**1**. However, the first node N**1** is coupled between the first and second capacitors CA**1** and CA**2** coupled in series. Hence, the voltage change is applied in the ratio "C'" as expressed in following equation:

$$C' = \frac{CA1}{CA1 + CA2} \tag{2}$$

where CA**1** represents the capacitance of the first capacitor C**1**, and CA**2** represents the capacitance of the second capacitor C**2**. As a consequence, "C'(DATA−Vth−Voled_anode)" is applied to the first node N**1**, and thus the voltage of the first node N**1** is changed to "DATA−C'(DATA−Vth−Voled_anode)". Meanwhile, the changed voltage of the first node N**1** is expressed in following equation with CA**1** and CA**2**:

$$\frac{\mathrm{DATA} \times CA2 + CA1(Vth + Voledanode)}{CA1 + CA2} \tag{3}$$

[0054] Also, the drain-source current Ids of the driving TFT DT supplied to the organic light emitting diode OLED is expressed by the following equation:

$$I_{ds} = k' \cdot (V_{gs} - V_{th})^2 \tag{4}$$

where k'represents a proportionality coefficient determined by the structure and physical properties of the driving TFT

DT, depending on the electron mobility of the driving TFT DT, channel width, channel length, etc. Vgs represents the voltage difference between the gate and source electrodes of the driving TFT DT, and Vth represents the threshold voltage of the driving TFT DT. 'Vgs-Vth' during the fourth period t4 is as expressed in the following equation:

$$Vgs - Vth = \left[\frac{\mathrm{DATA} \times CA2 + CA1(Vth + Voledanode)}{CA1 + CA2} - Voledanode\right] - Vth \quad (5)$$

[0055] To sum up Equation 5, the drain-source current Ids of the driving TFT DT is derived as expressed in the following equation:

$$Vgs - Vth = \left[\frac{\mathrm{DATA} \times CA2}{CA1 + CA2} - \frac{CA2(Voledanode + Vth)}{CA1 + CA2}\right] \quad (6)$$

[0056] With reference to equation 6, "Vgs-Vth" depends on the capacitance CA1 of the first capacitor C1 and the capacitance CA2 of the second capacitor C2. The larger the capacitance CA1 of the first capacitor C1 is, the larger "CA1+CA2" of the equation 6 becomes, and the smaller "Vth" of the equation 6 becomes. In this case, "CA2(Voled_anode+Vth)/(CA1+CA2)" of the equation 6 becomes smaller, and thus the compensation capability of the threshold voltage Vth of the driving TFT DT becomes higher. Also, the larger the capacitance CA2 of the second capacitor C2 is, the larger "DATA×CA2" of the equation 6 becomes and the larger "DATA" of the equation 6 becomes. That is, the drain-source current Ids of the driving TFT DT becomes wider because the range of "DATA" becomes wider. Therefore, the range of the luminance of the organic light emitting diode OLED becomes wider. And thus, the range of the pixel luminance which a pixel P represents becomes wider. Finally, the larger the capacitance CA1 of the first capacitor C1 is, higher the compensation capability of the threshold voltage Vth of the driving TFT DT becomes. Also, the larger the capacitance CA2 of the second capacitor C2 is, wider the range of the pixel luminance becomes. The capacitance CA1 of the first capacitor C1 and the capacitance CA2 of the second capacitor C2 are designed in consideration of the compensation capability of the threshold value Vth and the range of the pixel luminance

[0057] Fifth, during the fifth period t5, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. 3. Also, during the fourth period t5, the emission signal EM having the gate low voltage VGL is supplied through the emission line EML as shown in FIG. 3.

[0058] With reference to FIG. 5E, the first TFT T1 is turned off by the scan signal SCAN having the gate low voltage VGL. Therefore, the first node N1 is not coupled to the data line DL. The second TFT T2 is turned off by the emission signal EM having the gate low voltage VGL. Therefore, the second node N2 is no longer coupled to the third node N3. The third TFT T3 and the fourth TFT T4 are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N2 and the third node N3 is not coupled to the second reference voltage line REF2. Finally, the drain-source current Ids of the driving TFT DT is retained as in equation 6 during the fifth period t5.

[0059] As described above, the pixel P according to the first exemplary embodiment is driven as a source follower method that senses the threshold voltage Vth of the driving TFT DT by using the second node N2 coupled to the source electrode of the driving TFT DT. By driving using a source follower method, the pixel P according to the first exemplary embodiment initializes the first node N1 to the first reference voltage REF1 and the second node N2 and the third node N3 to the second reference voltage REF2 during the first period t1. The second reference voltage REF2 is set to a voltage lower than a difference voltage between the first reference voltage REF1 and the threshold voltage Vth of the driving TFT DT. In this case, the first reference voltage REF1 and the second reference voltage REF2 may be designed based on the threshold voltage Vth of the driving TFT DT equal to or higher than 0V. As a result, the pixel P according to the first exemplary embodiment may sense the threshold voltage Vth of the driving TFT DT because a voltage difference Vgs between a gate node Ng and a source node Ns of the driving TFT DT can be controlled to be greater than the threshold voltage Vth even though the threshold voltage Vth is shifted to a negative voltage. A negative shift refers to shifting the threshold voltage Vth of the driving TFT DT to a voltage lower than 0 V when the driving TFT DT is implemented as an N-type MOSFET. The negative shift usually occurs when a semiconductor layer of the driving TFT DT is formed of an oxide.

[0060] Also, the pixel P according to the first exemplary embodiment compensates the threshold voltage Vth of the driving TFT DT by using the second node N2 and the third node N3 during the fourth period t4. "Voled_anode" that corresponds to the voltage of the second node N2 and the voltage of the third node N3 may include a variation of the threshold voltage Vth of the driving TFT DT because the second node N2 and the third node N3 are coupled to the organic light emitting diode OLED during the fourth period t4. Also, "Voled_anode" may include a variation of the low-potential voltage VSS which is caused by emitting the organic light emitting diode OLED. Therefore, the pixel P according to the first exemplary embodiment may compensate the variation of the threshold voltage Vth of the driving TFT DT and the variation of the low-potential voltage VSS.

[0061] Also, the pixel P according to the first exemplary embodiment may control the second period t2 that is a period of sensing the threshold voltage Vth of the driving TFT DT as several horizontal periods or dozens of horizontal periods. Therefore, the first exemplary embodiment may sense the threshold voltage Vth of the driving TFT DT accurately during the second period t2 even though the display panel is driven at high speed such as a frame frequency of 240 Hz or more.

[0062] Furthermore, according to the first exemplary embodiment, the high-potential voltage VDD may be dropped due to emission of the organic light emitting diode OLED by the drain-source current Ids of the driving TFT DT during the fourth and fifth periods t4, t5. However, the pixel P according to the first exemplary embodiment may be apply a voltage drop of the high-potential voltage VDD to the first node N1 when the second capacitor C2 is coupled between the first node N1 and the high-potential voltage line VDDL. Therefore, the pixel P according to the first exemplary embodiment may be compensate a voltage drop of the high-potential voltage VDD.

[0063] FIG. **6** is a circuit diagram of a pixel P according to a second exemplary embodiment. Referring to FIG. **6**, the pixel P according to the second exemplary embodiment comprises a driving TFT DT, an organic light emitting diode OLED, a control circuit, and capacitors. The control circuit includes a first TFT T**1**, and an initialization control circuit ICC. The initialization control circuit ICC includes second to fourth TFT T**2**~T**4**. The capacitors include a first capacitor C**1** and a second capacitor C**2**.

[0064] The pixel P according to the second exemplary embodiment is substantially same as the pixel P according to the first exemplary embodiment as shown in FIG. **2**. Hence, descriptions of the driving TFT DT, the organic light emitting diode OLED, the first to third TFTs T**1**, T**2**, and T**3**, and the first and second capacitors C**1**, C**2** will be omitted.

[0065] With reference to FIG. **6**, the fourth TFT T**4** is a second initialization TFT which initializes the third node N**3** to a second reference voltage REF**2** supplied through a second reference voltage line REFL**2** in response to an initialization signal INI supplied through an initialization line IL. A gate electrode of the third TFT T**4** is coupled to the initialization line IL, a source electrode thereof is coupled to the second reference voltage line REFL**2**, and a drain electrode thereof is the third node N**3**.

[0066] An initialization signal INI, a scan signal SCAN, an emission signal EM, and a data voltage DATA that are supplied to the pixel P according to the second exemplary is substantially same as described in FIG. **3**. Also, voltage changes of the first to third nodes N**1**, N**2**, N**3** will be described with reference to FIGS. **7**, **8**A to **8**E.

[0067] FIG. **7** is a table showing changes in the voltages of nodes of a pixel according to a second exemplary embodiment of the present invention. FIGS. **8**A to **8**E are a circuit diagram of a pixel according to a second exemplary embodiment of the present invention during first to fifth periods. An operation method of the pixel P according to the second exemplary embodiment will be described in the below with reference to FIGS. **3**, **7**, and **8**A to **8**E.

[0068] First, during the first period t**1**, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate high voltage VGH is supplied through the initialization line IL as shown in FIG. **3**. Also, during the first period t**1**, the emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. **3**.

[0069] With reference to FIG. **8**A, the first TFT T**1** is turned off by the scan signal SCAN having the gate low voltage VGL. The second TFT T**2** is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N**2** is coupled to the third node N**3**. The third TFT T**3** is turned on in response to the initialization signal INI having the gate high voltage VGH. Therefore, the first node N**1** is coupled to the first reference voltage line REFL**1**. The fourth TFT T**4** is turned on in response to the initialization signal INI having the gate high voltage VGH. Therefore, the third node N**3** is coupled to the second reference voltage line REF**2**.

[0070] Finally, the voltage of the first node N**1** is initialized to the first reference voltage REF**1** since the third TFT T**3** is turned on. The voltage of the second node N**2** is initialized to the second reference voltage REF**2** since the second TFT T**2** is turned on. The voltage of the third node N**3** is initialized to the second reference voltage REF**2** since the fourth TFT T**4** is turned on.

[0071] Meanwhile, the operation method of the pixel P according to the second exemplary embodiment is substantially same as the first exemplary embodiment described with reference to FIGS. **3**, **4**, and **5**A to **5**E. Therefore, the operation method of the pixel P according to the second exemplary embodiment during the second to fifth periods will be omitted.

[0072] FIG. **9** is a circuit diagram of a pixel P according to a third exemplary embodiment. Referring to FIG. **9**, the pixel P according to the third exemplary embodiment comprises a driving TFT DT, an organic light emitting diode OLED, a control circuit, and capacitors. The control circuit includes a first TFT T**1** and an initialization control circuit ICC. The initialization control circuit ICC includes second to fourth TFT T**2** through T**4**. The capacitors include a first capacitor C**1** and a second capacitor C**2**.

[0073] The pixel P according to the second exemplary embodiment is substantially same as the pixel P according to the first exemplary embodiment as shown in FIG. **2**. Hence, descriptions of the driving TFT DT, the organic light emitting diode OLED, the first to third TFTs T**1**, T**2**, and T**3**, and the first capacitor C**1** will be omitted.

[0074] With reference to FIG. **9**, the fourth TFT T**4** is a second initialization TFT which initializes the third node N**3** to a second reference voltage REF**2** supplied through a second reference voltage line REFL**2** in response to an initialization signal INI supplied through the initialization line IL. A gate electrode of the third TFT T**4** is coupled to the initialization line IL, a source electrode thereof is coupled to the second reference voltage line REFL**2**, and a drain electrode thereof is the third node N**3**.

[0075] The second capacitor C**2** is coupled between the third node N**3** and the second reference voltage line REFL**2**. In this case, the second capacitor C**2** stores a differential voltage between a voltage at the third node N**3** and the second reference voltage REF**2**. Or, the second capacitor C**2** may be coupled between the third node N**3** and the first reference voltage line REFL**1**. In this case, the second capacitor C**2** stores a differential voltage between a voltage at the third node N**3** and the first reference voltage REF**1**. Alternatively, the second capacitor c**2** is coupled between the third node N**3** and the high-potential voltage line VDDL. In this case, the second capacitor C**2** stores a differential voltage between a voltage at the third node N**3** and the high-potential voltage VDD.

[0076] An initialization signal INI, a scan signal SCAN, an emission signal EM, and a data voltage DATA that are supplied to the pixel P according to the third exemplary is substantially same as described in FIG. **3**. Also, voltage changes of the first to third nodes N**1**, N**2**, N**3** will be described with reference to FIGS. **10**, **11**A to **11**E.

[0077] FIG. **10** is a table showing changes in the voltages of nodes of a pixel according to a third exemplary embodiment. FIGS. **11**A to **11**E are a circuit diagram of a pixel according to a third exemplary embodiment of the present invention during first to fifth periods. An operation method of the pixel P according to the third exemplary embodiment will be described in the below with reference to FIGS. **3**, **10**, and **11**A to **11**E.

[0078] First, during the first period t**1**, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate high voltage VGH is supplied through the initialization line IL as shown in FIG. **3**. Also, during the first period t**1**, the

emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. **3**.

[0079] With reference to FIG. **11**A, the first TFT T**1** is turned off by the scan signal SCAN having the gate low voltage VGL. The second TFT T**2** is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N**2** is coupled to the third node N**3**. The third TFT T**3** is turned on in response to the initialization signal INI having the gate high voltage VGH. Therefore, the first node N**1** is coupled to the first reference voltage line REFL**1**. The fourth TFT T**4** is turned on in response to the initialization signal INI having the gate high voltage VGH. Therefore, the third node N**3** is coupled to the second reference voltage line REF**2**.

[0080] Finally, the voltage of the first node N**1** is initialized to the first reference voltage REF**1** since the third TFT T**3** is turned on. The voltage of the second node N**2** is initialized to the second reference voltage REF**2** since the second TFT T**2** is turned on. The voltage of the third node N**3** is initialized to the second reference voltage REF**2** since the fourth TFT T**4** is turned on.

[0081] Second, during the second period t**2**, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. **3**. Also, during the second period t**2**, the emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. **3**.

[0082] With reference to FIG. **11**B, the first TFT T**1** is turned off by the scan signal SCAN having the gate low voltage VGL. The second TFT T**2** is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N**2** is coupled to the third node N**3**. The third TFT T**3** and the fourth TFT T**4** are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N**2** and the third node N**3** is no longer coupled to the second reference voltage line REF**2**. Meanwhile, the second node N**2** and the third node N**3** have substantially the same potential since the second TFT T**2** is turned on.

[0083] Because the voltage difference Vgs between the gate and source electrodes of the driving TFT DT is greater than the threshold voltage Vth, the driving TFT DT forms a current path until the voltage difference Vgs between the gate and source electrodes reaches the threshold voltage Vth. Accordingly, the voltage of the second node N**2** rises up. Also, the voltage of the third node N**3** rises up since the second node N**2** is coupled to the third node N**3**. Meanwhile, the voltage change of the third node N**3** is applied to the first node N**1** by the cap boosting of the first capacitor C**1**. If the voltage of the first node N**1** which the voltage change of the third node N**3** is applied to is "A" voltage, the voltage of the second node N**2** rises up to a differential voltage A−Vth between the voltage A of the first node N**1** and the threshold voltage Vth of the driving TFT DT. Also, the voltage of the third node N**3** rises up to a differential voltage A−Vth between the voltage A of the first node N**1** and the threshold voltage Vth of the driving TFT DT since the second node N**2** is coupled to the third node N**3**. "A" voltage may be "REF**1**+α". Finally, the threshold voltage Vth of the driving TFT DT may be stored to the first capacitor C**1** during the second period t**2**.

[0084] Third, during the third period t**3**, the scan signal SCAN having the gate high voltage VGH is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. **3**. Also, during the third period t**3**, the emission signal EM having the gate low voltage VGL is supplied through the emission line EML as shown in FIG. **3**.

[0085] With reference to FIG. **11**C, the first TFT T**1** is turned on in response to the scan signal SCAN having the gate high voltage VGH. Therefore, the first node N**1** is coupled to the data line DL. The second TFT T**2** is turned off by the emission signal EM having the gate low voltage VGL. Therefore, the second node N**2** is no longer coupled to the third node N**3**. The third TFT T**3** and the fourth TFT T**4** are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N**2** and the third node N**3** is not coupled to the second reference voltage line REF**2**. Meanwhile, the data voltage DATA of the data line is supplied to the first node N**1** since the first TFT T**1** is turned on. The third node N**3** is on the floating state since the second TFT T**2** is turned off. The floating state refers to a state on which no voltage is supplied to a node, so the node on the floating state affects voltage change of an adjacent node easily.

[0086] The voltage change of the first node N**1** is applied to the third node N**3** since the third node N**3** is on the floating state during the third period t**3**. "A−DATA" corresponding to the voltage change of the first node N**1** is applied to the third node N**3**. However, the third node N**3** is coupled between the first and second capacitors CA**1** and CA**2** coupled in series. Hence, the voltage change is applied in the ratio "C'" as expressed in the equation 2. Therefore, "C'(A−DATA)" is applied to the third node, and the voltage of the third node N**3** is changed to "A−Vth−C'(A−DATA)".

[0087] Fourth, during the fourth period t**4**, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. **3**. Also, during the fourth period t**4**, the emission signal EM having the gate high voltage VGH is supplied through the emission line EML as shown in FIG. **3**.

[0088] With reference to FIG. **11**D, the first TFT T**1** is turned off by the scan signal SCAN having the gate low voltage VGL. Therefore, the first node N**1** is no longer coupled to the data line DL. The second TFT T**2** is turned on in response to the emission signal EM having the gate high voltage VGH. Therefore, the second node N**2** is coupled to the third node N**3**. The third TFT T**3** and the fourth TFT T**4** are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N**2** and the third node N**3** is not coupled to the second reference voltage line REF**2**. Meanwhile, the first node N**1** is on the floating state since the first TFT T**1** and the third TFT T**3** are turned off. The second node N**2** and the third node N**3** are at substantially the same potential since the second TFT T**2** is turned on.

[0089] The voltage of the second node N**2** is changed to "Voled_anode" due to the drain-source current Ids of the driving TFT DT according to the voltage of the first node N**1**. Also, the voltage of the third node N**3** is changed to "Voled_anode" because the second node N**2** is coupled to the third node N**3** since the second TFT T**2** is turned on.

[0090] The voltage change of the third node N**3** is applied to the first node N**1** by the first capacitor C**1** because the first node N**1** is on the floating state during the fourth period t**4**. Therefore, the voltage change of the third node N**3**, "{A−Vth−C'(A−DATA)}−Voled_anode" is applied to the first

node N1. As a consequence, the voltage of the first node N1 is changed to "DATA−{A−Vth−C'(A−DATA)−Voled_anode}".

[0091] The changed voltage of the first node N1 is expressed in following equation:

$$Vgs-Vth=[\text{DATA}-(A-Vth-C'(A-\text{DATA})-\text{Voledanode})-\text{Voledanode}]-Vth \quad (7)$$

[0092] To sum up Equation 7, the drain-source current Ids of the driving TFT DT is derived as expressed in the following equation:

$$I_{ds}=k'[(1-C')\cdot(\text{DATA}-A)]^2 \quad (8)$$

[0093] With reference to equation 8, the drain-source current Ids does not depend on the threshold voltage Vth of the driving TFT DT during the fourth period t4. That is, the threshold voltage Vth of the driving TFT DT may be compensated.

[0094] Fifth, during the fifth period t5, the scan signal SCAN having the gate low voltage VGL is supplied through the scan line SL, and the initialization signal INI having the gate low voltage VGL is supplied through the initialization line IL as shown in FIG. 3. Also, during the fourth period t5, the emission signal EM having the gate low voltage VGL is supplied through the emission line EML as shown in FIG. 3.

[0095] With reference to FIG. 11E, the first TFT T1 is turned off by the scan signal SCAN having the gate low voltage VGL. Therefore, the first node N1 is not coupled to the data line DL. The second TFT T2 is turned off by the emission signal EM having the gate low voltage VGL. Therefore, the second node N2 is no longer coupled to the third node N3. The third TFT T3 and the fourth TFT T4 are turned off by the initialization signal INI having the gate low voltage VGL. Therefore, each of the second node N2 and the third node N3 is not coupled to the second reference voltage line REF2. Finally, the drain-source current Ids of the driving TFT DT is retained as in equation 8 during the fifth period t5.

[0096] As described above, the pixel P according to the third exemplary embodiment is driven as a source follower method that senses the threshold voltage Vth of the driving TFT DT by using the second node N2 coupled to the source electrode of the driving TFT DT. By driving using the source follower method, the pixel P according to the third exemplary embodiment initializes the first node N1 to the first reference voltage REF1 and the second node N2 and the third node N3 to the second reference voltage REF2 during the first period t1. The second reference voltage REF2 is set to a voltage lower than a difference voltage between the first reference voltage REF1 and the threshold voltage Vth of the driving TFT DT. In this case, the first reference voltage REF1 and the second reference voltage REF2 may be designed based on the threshold voltage Vth of the driving TFT DT equal to or higher than 0V. As a result, the pixel P according to the third exemplary embodiment may sense the threshold voltage Vth of the driving TFT DT because a voltage difference Vgs between a gate node Ng and a source node Ns of the driving TFT DT can be controlled greater than the threshold voltage Vth even though the threshold voltage Vth is shifted to a negative voltage. A negative shift refers to shifting the threshold voltage Vth of the driving TFT DT to a voltage lower than 0 V when the driving TFT DT is implemented as an N-type MOSFET. The negative shift usually occurs when a semiconductor layer of the driving TFT DT is formed of an oxide.

[0097] Also, as can be noted in Equation (8), the drain-source current Ids of the driving TFT DT does not depend upon the threshold voltage Vth of the driving TFT DT. Hence, compared to the embodiments of FIGS. 2 and 6, the compensation of the threshold voltage can be performed more enhanced in the embodiment of FIG. 9.

[0098] Also, the pixel P according to the third exemplary embodiment compensates the threshold voltage Vth of the driving TFT DT by using the second node N2 and the third node N3 during the fourth period t4. "Voled_anode" that corresponds to the voltage of the second node N2 and the voltage of the third node N3 during the fourth period t4 may include a variation of the threshold voltage Vth of the driving TFT DT because the second node N2 and the third node N3 are coupled to the organic light emitting diode OLED during the fourth period t4. Also, "Voled_anode" may include a variation of the low-potential voltage VSS which is caused by emitting the organic light emitting diode OLED. Therefore, the pixel P according to the first exemplary embodiment may compensate the variation of the threshold voltage Vth of the driving TFT DT and the variation of the low-potential voltage VSS.

[0099] Furthermore, the pixel P according to the third exemplary embodiment may control the second period t2 that is a period of sensing the threshold voltage Vth of the driving TFT DT as several horizontal periods or dozens of horizontal periods. Therefore, the third exemplary embodiment may sense the threshold voltage Vth of the driving TFT DT accurately during the second period t2 even though the display panel is driven at high speed such as a frame frequency of 240 Hz or more.

[0100] FIG. 12 is a block diagram schematically showing an organic light emitting diode display device according to an exemplary embodiment. Referring to FIG. 12, the organic light emitting diode display device according to the exemplary embodiment comprises a display panel 10, a data driver 20, a scan driver 30, a timing controller 40, and a host system 50.

[0101] Data lines DL and scan lines SL crossing each other are formed on the display panel 10. Initialization lines IL and emission lines EML may be formed in parallel with the scan lines SL on the display panel 10. Also, pixels P are arranged in a matrix form on the display panel 10. Each of the pixels P of the display panel 10 is as described in conjunction with FIG. 2, FIG. 6, and FIG. 9.

[0102] The data driver 20 comprises a plurality of source drive ICs. The source drive ICs receive digital video data RGB from the timing controller 40. The source drive ICs convert the digital video data RGB into a gamma compensation voltage in response to a source timing control signal DCS from the timing controller 40 to generate data voltages and supply the data voltages to the data lines DL of the display panel 10 in synchronization with scan signals SCAN.

[0103] The scan driver 30 comprises a scan signal output part, an initialization signal output part, and an emission signal output part. The scan signal output part sequentially outputs the scan signals SCAN to the scan lines SL of the display panel 10. The initialization signal output part sequentially outputs initialization signals to the initialization lines IL. The emission signal output part sequentially outputs emission signals EM to the emission lines EML of the display panel 10. Detailed descriptions of the scan signal SCAN, the initialization signal INI, and the emission signal EM will be described in detail in conjunction with FIG. 3.

[0104] The timing controller 40 receives digital video data RGB from the host system 50 through a low voltage differential signaling (LVDS) interface, a transition minimized dif-

ferential signaling (TMDS) interface, etc. The timing controller **40** receives timing signals such as a vertical synchronization signal, a horizontal synchronization signal, a data enable signal, and a dot clock, and generates timing control signals for controlling operation timings of the data driver **20** and scan driver **30** based on the timing signals from the host system **50**. The timing control signals comprise a scan timing control signal for controlling the operation timing of the scan driver **30** and a data timing control signal for controlling the operation timing of the data driver **20**. The timing controller **40** outputs the scan timing control signal to the scan driver **30**, and outputs the data timing control signal and the digital video data RGB to the data driver **20**.

[0105] The display panel **10** may further comprise a power supply unit (not shown). The power supply unit supplies a high-potential voltage VDD, a low-potential voltage VSS, a first reference voltage REF**1**, and a second reference voltage REF**2** to the display panel **10**. Further, the power supply unit supplies a gate high voltage VGH and a gate low voltage VGL to the scan driver **30**.

[0106] The embodiments described herein are driven using a source follower that senses the threshold voltage Vth of the driving TFT DT by using the second node N**2** coupled to the source electrode of the driving TFT DT. By driving as the source follower, the embodiments described herein initialize the first node N**1** to the first reference voltage REF**1** and the second node N**2**, and the third node N**3** to the second reference voltage REF**2** during the first period t**1** (i.e., an initialization period). The second reference voltage REF**2** is set to a voltage lower than a difference voltage between the first reference voltage REF**1** and the threshold voltage Vth of the driving TFT DT. As a result, the embodiments described herein may sense the threshold voltage Vth of the driving TFT DT because a voltage difference Vgs between a gate node Ng and a source node Ns of the driving TFT DT can be controlled to be greater than the threshold voltage Vth even though the threshold voltage Vth is shifted to a negative voltage.

[0107] Also, the embodiments described herein compensate the threshold voltage Vth of the driving TFT DT by using the second node N**2** and the third node N**3** during the fourth period t**4**. "Voled_anode" that corresponds to the voltage of the second node N**2** and the voltage of the third node N**3** may include a variation of the threshold voltage Vth of the driving TFT DT because the second node N**2** and the third node N**3** are coupled to the organic light emitting diode OLED during the fourth period t**4**. Also, "Voled_anode" may include a variation of the low-potential voltage VSS which is caused by emitting the organic light emitting diode OLED. Therefore, the embodiments described herein may compensate the variation of the threshold voltage Vth of the driving TFT DT and the variation of the low-potential voltage VSS.

[0108] Also, the embodiments described herein may extend the second period t**2** corresponding to a period of sensing the threshold voltage Vth of the driving TFT DT to several horizontal periods or dozens of horizontal periods. Therefore, the embodiments described herein may sense the threshold voltage Vth of the driving TFT DT more accurately during the second period t**2** even though the display panel is driven at a high speed (e.g., a frame frequency of 240 Hz or more).

[0109] Furthermore, according to the first exemplary embodiment, the high-potential voltage VDD may be dropped due to emission of the organic light emitting diode OLED by the drain-source current Ids of the driving TFT DT during the fourth and fifth periods t**4**, t**5**. However, the pixel P according to the first exemplary embodiment may apply a voltage drop of the high-potential voltage VDD to the first node N**1** when the second capacitor C**2** is coupled between the first node N**1** and the high-potential voltage line VDDL. Therefore, the pixel P according to the first exemplary embodiment may compensate a voltage drop of the high-potential voltage VDD.

[0110] Although the embodiments of this application have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments of this application can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

1. An organic light emitting diode display device comprising a plurality of pixels arranged in a matrix form, each of the pixels comprising:

a driving thin film transistor (TFT) including a gate electrode coupled to a first node, a source electrode coupled to a second node, and a drain electrode coupled to a high-potential voltage line;

an organic light emitting diode between the second node and a low-potential voltage line;

a first TFT configured to connect a data line to the first node during a data voltage supply period of a frame period;

an initialization control circuit coupled between the first node and a first reference voltage line supplying a first reference voltage, the initialization control circuit further connected to a second node, a third node and a second reference voltage line supplying a second reference voltage, the initialization control circuit configured to initialize the first node to the first reference voltage, and the second and third nodes to a second reference voltage during an initialization period of the frame period preceding the data voltage supply period, the initialization control circuit comprising:

a second TFT including a gate electrode coupled to an emission line, a source electrode coupled to the third node, and a drain electrode coupled to the second node,

a third TFT including a gate electrode coupled to an initialization line for carrying an initialization signal to indicate the initialization period, a source electrode coupled to the first reference voltage line supplying the first reference voltage, and a drain electrode coupled to the first node, and

a fourth TFT including a gate electrode coupled to the initialization line, a source electrode coupled to the second reference voltage line supplying the second reference voltage, and a drain electrode coupled to the third node; and

a first capacitor coupled between the first node and the third node, the first capacitor configured to store a voltage difference between the first node and the third node during the initialization period, and change a voltage level of the first node based on a voltage level of the third

node in a threshold voltage sensing period between the initialization period and the data voltage supply period.

2. The organic light emitting diode display device of claim **1**, wherein each of the pixels further comprising a second capacitor coupled between the third node and the second reference voltage line supplying the second reference voltage.

* * * * *

专利名称(译)	有机发光二极管显示装置的驱动晶体管中的阈值电压的补偿		
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[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
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发明人	BAE, NAYOUNG YOON, JOONGSUN SHIN, MINJAE		
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摘要(译)

该有机发光二极管显示装置包括显示面板，多个像素以矩阵形式排列，每个像素包括：驱动TFT，包括耦合到第一节点的栅电极，耦合到第二节点的源电极，以及漏极连接到高电位电压线;有机发光二极管，包括耦合到第二节点的阳极和耦合到低电势电压线的阴极;第一TFT响应扫描信号向第一节点提供数据电压;初始化控制电路，响应初始化信号和发射信号，将第一节点初始化为第一参考电压，将第二节点或第三节点初始化为第二参考电压;和电容器。